DESIGN OF SIGE HBT POWER AMPLIFIERS FOR MICROWAVE RADAR APPLICATIONS

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DESIGN OF SIGE HBT POWER AMPLIFIERS FOR MICROWAVE RADAR APPLICATIONS

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To my beautiful boys, George and Gabriel, for daily helping me see the world through new eyes.

To my wife, Amber, for being my best friend.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

This dissertation explores the design of Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) power amplifiers for radar applications at X-Band (8-12 GHz) and above. As successive generations of SiGe become faster and faster, they consequently experience decreasing breakdown voltages. This lack of breakdown voltage presents a fundamental challenge for power amplifiers to achieve necessary output power and efficiency parameters for the systems in which they operate. Novel techniques for increasing breakdown voltage as well as techniques for thermally optimizing power amplifier cells are investigated.

For X-Band power amplifiers, this dissertation covers:

1. A mixed breakdown cascode architecture for increased breakdown voltage in SiGe (Chapter II, also published in [1]).
2. A high-gain two-stage power amplifier operating from 8.5 to 10.5 GHz with a nominal output power of 20 dBm and a Power-Added-Efficiency (PAE) of 25% (Chapter III, also published in [2], [3], and [4]).
3. A high power SiGe amplifier with a near one Watt output power (Chapter IV, also published in [5]).

Additionally, techniques for thermally modeling and optimizing power amplifier structures in commercially available design kits are presented. For thermal optimizing and modeling the dissertation covers:

1. Analysis of thermal coupling between adjacent devices through the use of infrared imagery (Chapter V, also published in [6]).
2. Modeling and optimization techniques in commercially available software, exhibited through the thermal balance of a multi-transistor array (Chapter VI, also accepted for publication in *IEEE Transactions on Electron Devices*).

CHAPTER I

ORIGIN AND HISTORY OF PROBLEM: PHASED ARRAY RADARS, PAST, PRESENT, AND FUTURE

1.1 A Brief History of Radar

RAdio Detecting And Ranging, more commonly known as RADAR, has its earliest roots in World War II Europe. The first military application of radar was employed by the Allied Forces as an early warning system against German bombers approaching England to drop their payloads [7]. These early systems consisted of stationary antennas driven with high power electro-magnetic devices called magnetrons which pulsed RF energy and "listened" back for echos from potential oncoming targets.

As time has progressed, so has the value and the complexity of radar systems. Radar is now used for commercial applications such as weather monitoring and prediction [8] as well as auto collision detection [9], and radar is still invaluable for many military uses. Mechanically movable antennas have been, and still are, employed to increase the viewable area of radar systems, but scanning rates are limited by the mass of the system, and are limited to hundreds of scans per minute. Electrically steer-able systems based upon arrays consisting of large numbers of radiators are capable of hundreds of scans per second over wide viewing areas [10].

As system architectures have advanced, so have the components. The magnetron has given way to vacuum tube based systems, which have now been replaced by higher reliability solid state systems which are used to steer phased array beams. Future trends in phased array radar are pushing for smaller, more compact solid state systems with an ultimate goal of putting all beam steering functions on a single chip [11].

1.2 Modern Day Phased Array Radars

Phased array radars are the current detection system of choice for military missile defense systems. With the ability to rapidly scan for single or multiple targets, determine those

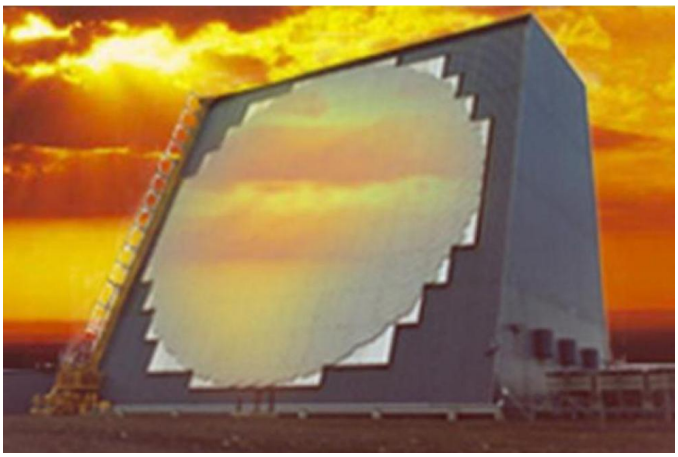

Figure 1: Photograph of large missile defense phased array radar in Alaska demonstrating two-dimensional tiling of radiators.

targets' trajectories, and assist with targeting and launching of intercepting missiles, phased array radars are ideal for both air and ground based missile defense systems [12]. Perhaps the most popularly known ground based phased array radar for this purpose is the Patriot system that was widely used in The Gulf War in the early 1990s to destroy Iraqi SCUD missiles [13]. The system consists of a transportable radar array in conjunction with a missile launching platform [14]. The rapid scanning capabilities of the phased array radar greatly improve the targeting capabilities of the missile, producing the spectacular missile kill shots seen by the general public on the evening news.

As opposed to the use of a parabolic antenna which focuses power onto a single transmit and receive radiator, phased arrays are made up of many individual radiators spaced at fractional intervals of the wavelength of operation in two spatial dimensions, as can be seen in Figure 1. Varying the phase of the signal applied to each radiator on transmit allows for coherent transmission of the radiated signal at varying angles of azimuth and elevation. Similarly on receive, phase delay allows for coherent recombination of the received signal that can then be processed at other points in the system [14].

1.2.1 Passive Phased Array Radars

Early ground based phased array systems, such as that employed by the Patriot, are known as passive phased arrays [15]. In such systems, multiple phase shifters are driven by a

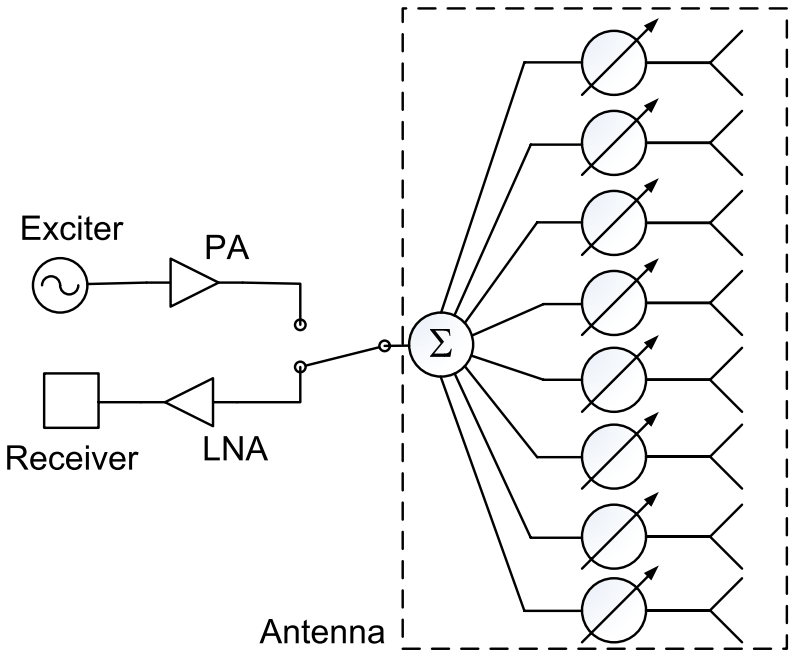

Figure 2: Block diagram of a passive phased array radar showing centralized amplification scheme.

single power amplifier on transmit and conversely, multiple phase shifters drive a single low noise amplifier on receive, as can be seen in Figure 2. Such systems, are easier to fabricate because of a more centralized architecture on transmit and receive [16], but they suffer from multiple detracting qualities. From a receiver sensitivity standpoint, the phase shifter located in front of the low noise amplifier degrades the overall system noise figure [17]. Similarly on transmit, having the phase shifter located after the power amplifier decreases overall system efficiency, since the power amplifier is located far away from the radiator and has to transmit through lossy series elements. The phase shifter in this architecture is also required to handle relatively high power levels. Such systems use phase shifter technologies based upon ferrites capable of handling high powers, which are generally large compared to lower power solid state phase shifters [18]. While the Patriot has over 5000 phase shifters, 16 phase shifters are driven by a single Power Amplifier (PA)/Low Noise Amplifier (LNA) pair [15]. From a reliability standpoint, these systems are unattractive since a failure in either amplifier path takes out a significant part of the array in terms of radiators.

1.2.2 Active Phased Array Radars

The successor to the Patriot, the THAAD system, is an active phased array radar system. As opposed to a passive system, each radiator has its own dedicated Transmit/Receive (T/R) module, as can be seen in Figure 3. The active system architecture has inherently improved noise figure and overall system efficiency since both transmit and receive amplifiers are located on the radiator side of the phase shifter [19]. Not only did THAAD increase the number of phase shifters by more than five over Patriot [20], but each phase shifter is dedicated to its own radiator. Thus, this architecture greatly improves the reliability of the overall system, since the loss of a single module represents a fraction of a percent of the entire operating array. The distributed amplifier architecture not only relaxes the power handling requirements on the phase shifters, but also greatly relaxes the required output power per amplifier by no longer being distributed over multiple radiators. Thus, THAAD's construction consists of full MMIC integration in the T/R modules. These modules consist of a discrete chip for each LNA, beam steering logic, phase shifter, and PA. The modules also contain the necessary circulators and switches for operation. An example of such a module can be seen in Figure 4. The output power of the Galium Arsenide (GaAs) final power amplifier used is approximately 40 dBm with over 40% Power Added Efficiency (PAE) [19].

1.2.3 Financial and Physical Drivers of Military Radar Systems

The two main driving factors for the array size for both Patriot and THAAD were 1) overall design cost and 2) system size and weight, which impacts its deploy-ability with available military transport vehicles and aircraft. The T/R module construction made up the vast majority of the design cost because of both individual part cost as well as assembly costs [19]. However, the T/R module size and weight was the main limiting factor in the ultimate size of the array due to transportation limits [20]. In attempts to lower both of these costs at the same time, integration of functionality on to fewer and potentially even one chip is the solution. Unfortunately, the power requirements of THAAD for transmit per module combined with the overall system integration does not lend itself to any existing technologies. Consequently, a new design paradigm for T/R modules is needed.

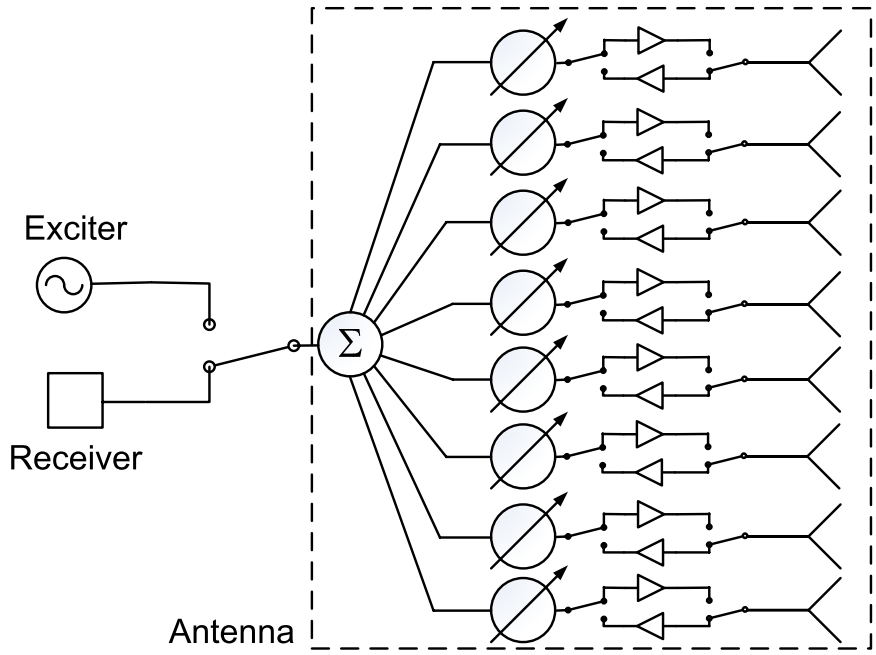

Figure 3: Block diagram of an active phased array radar showing distributed amplifier architecture.

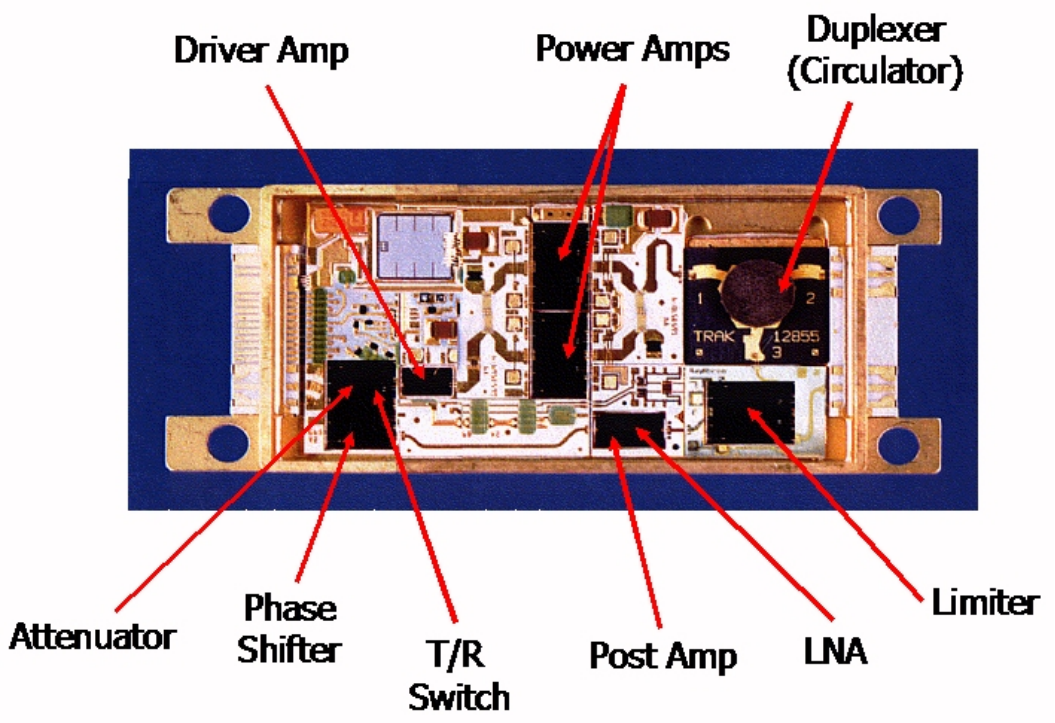

Figure 4: A Transmit/Receive module highlighting amplification, phase shifting, switching, and digital control functionality.

1.3 Down-sizing T/R Modules based upon FOM

For phased array radars, there are three main figures of merit (FOM). They are 1) the power-aperture product for search, 2) the power-aperture-gain product for track, and 3) the power-aperture-gain-squared product for track accuracy defined in [21], respectively, as:

$$FOM_{search} = P_{Avg}A \tag{1}$$

$$FOM_{track} = P_{Avg}AG \tag{2}$$

$$FOM_{trackaccuracy} = P_{Avg}AG^2 \tag{3}$$

where P_{Avg} is the average transmit power of the array, A is the aperture area of the array, and G is the gain of the antenna. In an active phased array, these terms are not necessarily independent. The power, aperture area, and gain of the entire array can be defined in terms of individual radiator elemental values as:

$$P = P_eN \tag{4}$$

$$A = A_eN \tag{5}$$

$$G = G_eN \simeq \frac{4\pi A_E}{\lambda^2}N \tag{6}$$

where P_e,A_e,G_e are the power, aperture area, and gain of a single radiating element, respectively. λ and N are the wavelength of operation and number of elements in the array. Substituting (4)-(6) back into (1)-(3) allows them to be rewritten as:

$$FOM_{search} = P_eA_eN^2 \tag{7}$$

$$FOM_{track} = P_eA_e^2\frac{4\pi}{\lambda^2}N^3 \tag{8}$$

Table 1: Design example from Mitchell and Wallace demonstrating available decrease in required system power as a function of elemental power at a fixed value of $PAG = 100$ dB(Wm^2).

P_e (Watts)	Array Area (m^2)	System Power (kiloWatts)	Number of Elements
100	5.8	468	4,680
10	12.6	100	10,000
.5	34	20	40,000
.01	126	26	2,600,000

$$FOM_{trackaccuracy} = P_e A_e^3 \left(\frac{4\pi}{\lambda^2}\right)^2 N^4 \tag{9}$$

Focusing on the track figure of merit (8), improvement can be made by increasing either the elemental power P_e, elemental aperture area A_e, or the number of elemental radiators N. Increasing P_e only allows for a linear increase in PAG, the track FOM, and at the same time linearly increases the amount of heat which must be dissipated from the array by heat exchangers. The heat exchangers represent a cost adder as well as a detractor from the overall weight budget of the system and is not an attractive solution. An increase in the aperture area provides a squared increase to PAG, however, increasing radiator spacing beyond much more than $\lambda/2$ will introduce unwanted grating lobes at extreme steering angles, undesirably reducing the available steer angles of the array. As opposed to the prior two changes, increasing the number of radiators not only improves the figure of merit by a cubed factor, but also has the additional advantage of decreasing the power per unit radiator, as well as drastically decreasing the power requirements of the entire array [22].

As can be seen in Table 1, overall system power requirements decrease drastically for a fixed value of PAG with only moderate increases in overall array area. However, it can also be seen that P_e can not be decreased to an arbitrarily small value, and for the application in question, an elemental power of 0.5 to 2 Watts is optimal. At the T/R module level, this allows for significantly decreased output power, but an increase in overall modules. The decrease in cost of a standard T/R module resultant from changing the

output power amplifier chip in the THAAD modules for one with lower output power is practically unnoticeable in quantity for cost. Additionally, simply trading out the power amplifier in the T/R module does not in any way decrease its overall weight. Since the size of the array is already predominantly set by system weight, with the lion's share of that attributable to the T/R module, this scheme is not feasible.

Exploiting the decrease in T/R module output power requires a new design methodology: system integration on chip. While a technology such as the currently used GaAs is quite capable of satisfying the mm-wave needs of a T/R module, digital logic is difficult to integrate in this technology, due to the lack of a complementary device for creating low loss, high speed circuits. However, a technology which easily integrates digital logic on chip with similar high frequency transistor performance is SiGe. The reduced power output specified by this analysis opens up the door for SiGe to perform full T/R system integration with the power amplifier included.

1.4 SiGe as a Millimeter Wave Technology

Silicon has long been the integrated circuit substrate of choice because of its ready availability, ease of handling, and the ease with which it produces a high quality dielectric, Silicon Dioxide. Consequently, the Silicon IC industry and its manufacturing capabilities have matured to the point where the production of Silicon circuits is very inexpensive. Unfortunately, the small bandgap of Silicon makes it a poor competitor in the millimeter-wave arena [23]. The desire to improve the frequency performance of Silicon has driven band gap engineering research and design with Silicon substrates.

The addition of Germanium to Silicon has its earliest roots with the original bipolar transistor patent by Kroemer [24], but it was not until the mid 1980s that acceptably low defect films of SiGe were generated [25]. The addition of Germanium to the base of a Silicon transistor, as shown in Figure 5, allows for tuning of the inherent Silicon bandgap, greatly increasing the operating frequency of the subsequent devices. Record setting performance in SiGe boasts cryogenic transistor f_T's of greater than 500 GHz in 4^{th} generation platforms [26]. While these transistors exhibit performance similar to and, in some cases, in excess of

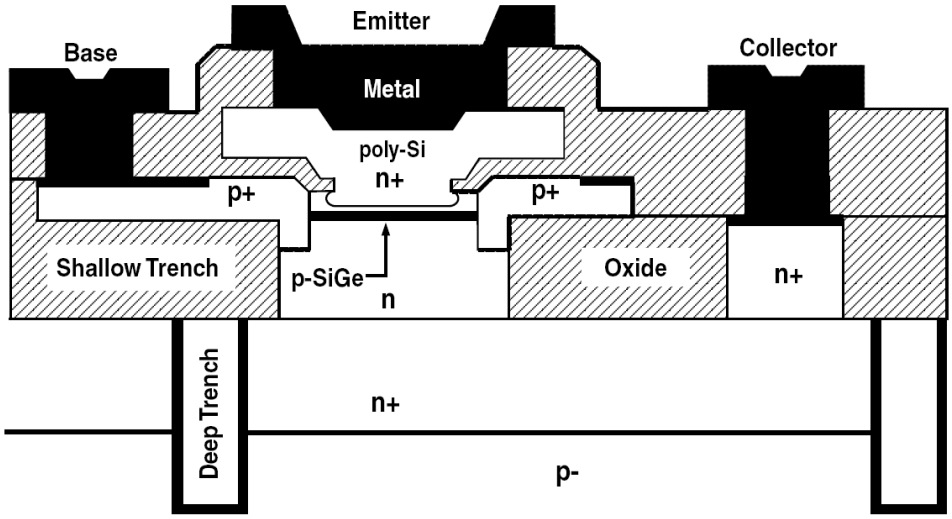

Figure 5: Cross section of an example SiGe HBT.

III-V technologies, the Silicon substrate can be processed in the same way as the mature Silicon processing environment, which offers the promise of ever decreasing wafer and chip costs. The bulk Silicon substrate offers the addition of CMOS devices as processing mask adders, bolstering the high frequency capability of the medium with a commercially available digital technology, on chip [27].

1.5 SiGe Power Amplifiers

SiGe has made large strides in low power mm-wave building blocks such as LNAs and Voltage Controlled Oscillators (VCOs) at frequencies from a few gigahertz to 77 GHz and above because of its good noise characteristics [28]. Additionally, current advancements in high speed A/D's in SiGe make it an excellent choice of substrate for T/R module integration. The main lacking component available for on chip designs is the power amplifier. This is due to SiGe's low breakdown voltages compared to other III-V technologies. Breakdown voltage in SiGe is inherently related to peak f_T of operation through the $BV_{CEO} \times f_T$ product, which is commonly known as the Johnson Limit; a constant [27]. While SiGe has f_T values over 500 GHz, the need for high breakdown voltages in power amplifier design has seen only relatively high power PAs designed at low frequencies in this technology. An example of this is the 1.9 GHz frequency range for the cellular phone market, where breakdown voltages are 8-9 volts, nearly twice the standard DC supply voltage in that application [29]. Other power amplifiers have been designed at 5.8 GHz [30], X-Band [31], and above [32], but all of these have been at modest powers not exceeding one half of a Watt [33]. An increase in breakdown voltage in SiGe can assist greatly with its usage for power amplifiers.

1.6 Motivation for Dissertation

With digital and high frequency capabilities, SiGe is an ideal substrate for module integration. Reduced power requirements from 40 dBm to 30 dBm as a result of the new radar design paradigm allows for full system T/R design in SiGe. Phase shifting, low noise amplification, and digital logic can all be implemented in SiGe to comparable performance levels of competing technologies. Of all of the T/R module functionality necessary, the final stage power amplifier presents the greatest challenge. This dissertation aims to present novel

techniques for improving breakdown voltages and thermal analysis of SiGe power amplifiers for X-Band and above.

1.7 Organization of Dissertation

Chapter II (also published in [1]) introduces a variation on the well known cascode amplifier structure. Employing differing speed and breakdown voltage transistors available in SiGe, increased breakdown voltage and gain are achieved simultaneously. Load pull results on the initial power amplifier structures are presented which show greater than 40% PAE at X-Band.

Chapter III (also published in [2], [3], and [4]) is an implementation of the techniques presented in [1] to achieve a two stage power amplifier with greater than 40 dB of gain, 25% PAE and 20 dBm of output power across the design band of 8.5 GHz to 10.5 GHz. The amplifier was fabricated in IBM's 8HP technology and occupies a space of 1.1 mm x 1.2 mm with pads.

Chapter IV (also published in [5]) is a high power implementation of the mixed breakdown cascode architecture in the form of a single stage, 850 mW X-Band amplifier in SiGe. Load pull results are presented at 9.5 GHz which show impedance values for the input and output of the structure with a gain of 11 dB and a PAE of 18%. Chip on board results further corroborate the output power and efficiency results. The resulting die size including pads is 1.5 mm x 3 mm.

Chapter V (also published in [6]) presents techniques for thermal analysis of arrays of transistors commonly used in SiGe power amplifier cells. Varied placement and orientations are studied and imaged with thermal imaging equipment to determine thermal coupling between adjacent devices. It is shown that for adjacent devices in SiGe technology, it is feasible to use lumped element analysis to describe their thermal coupling.

Chapter VI (also submitted for publication in *IEEE Transactions on Electron Devices*) presents a model for use in a thermal network which can easily be implemented into commercial SiGe design and layout tools. Using the finding in [6], a power amplifier cell is

optimized for device spacing to minimize thermal gradients across the structure. Minimally and optimally spaced cells are designed and fabricated to demonstrate the thermal differences between the two layouts.

Chapter VII concludes the dissertation with a discussion of contributions and possible future work.

CHAPTER II

MIXED BREAKDOWN CASCODE POWER AMPLIFIERS

2.1 Introduction

Collector doping variations [34] and other techniques have been used to increase breakdown voltages in SiGe, but are in general relegated to experimentation and not available in commercially available processes. Increased operating voltage through the use of Common Base (CB) amplifiers has been shown [35], but with relatively poor power gain for the PA. A novel change to the cascode architecture for SiGe power amplifiers is presented. This method shows greater than twice the Collector-Emitter Breakdown Voltage (BV_{CEO}) operating voltage along with excellent gain through mixed breakdown voltage transistor operation.

2.2 Improved Breakdown Voltages

It has been shown in [36] that by driving a SiGe HBT with a forced I_E (as opposed to a forced I_B) that the breakdown characteristics of the device can be increased from the BV_{CEO} value to nearly that of the Collector-Base Breakdown Voltage (BV_{CBO}) voltage, which is generally twice that of the BV_{CEO} voltage, as is seen in Figure 6. To operate a device as an amplifier suggests that it should be operated in the Common Base configuration shown in Figure 7(b) as opposed to the more widely used Common-Emitter (CE) configuration shown in Figure 7(a). Incorporating the two together provides for a CE/CB hybrid, the commonly known cascode configuration shown in Figure 7(c).

In the cascode architecture, the CE operated device not only acts as the gain providing element, but also acts to force an I_E for the CB device, providing the aforementioned increased breakdown voltage. The output characteristic of a second generation SiGe HBT with a 45 GHz peak f_T operated in a CE mode is shown in Figure 8. Breakdown is seen to occur in this device at below 3 Volts, whereas the same device run as the CB portion of a cascode amplifier shown in Figure 9 exhibits a breakdown voltage of nearly 8 Volts.

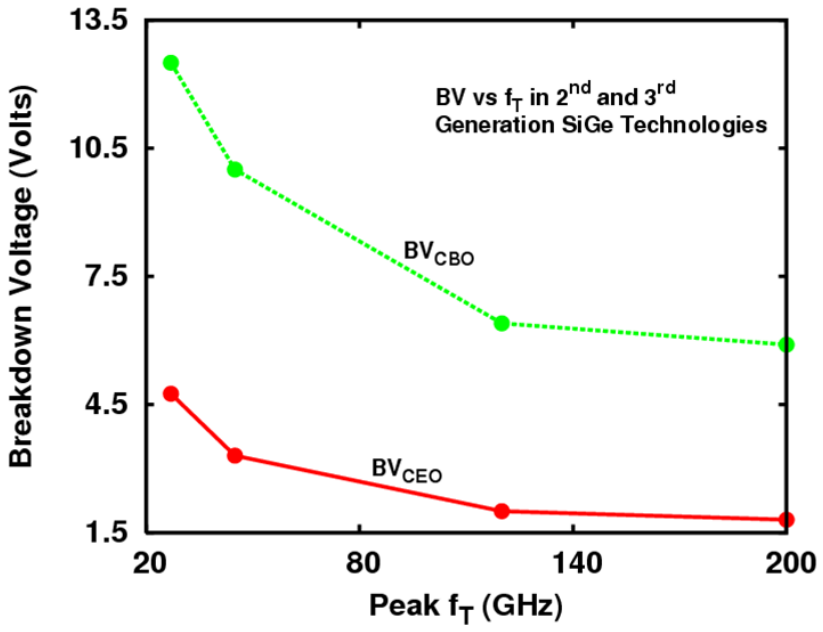

Figure 6: Collector-Emitter Breakdown Voltage (BV_{CEO}) and Collector-Base Breakdown Voltage (BV_{CBO}) vs. peak f_T in second and third generation SiGe technologies.

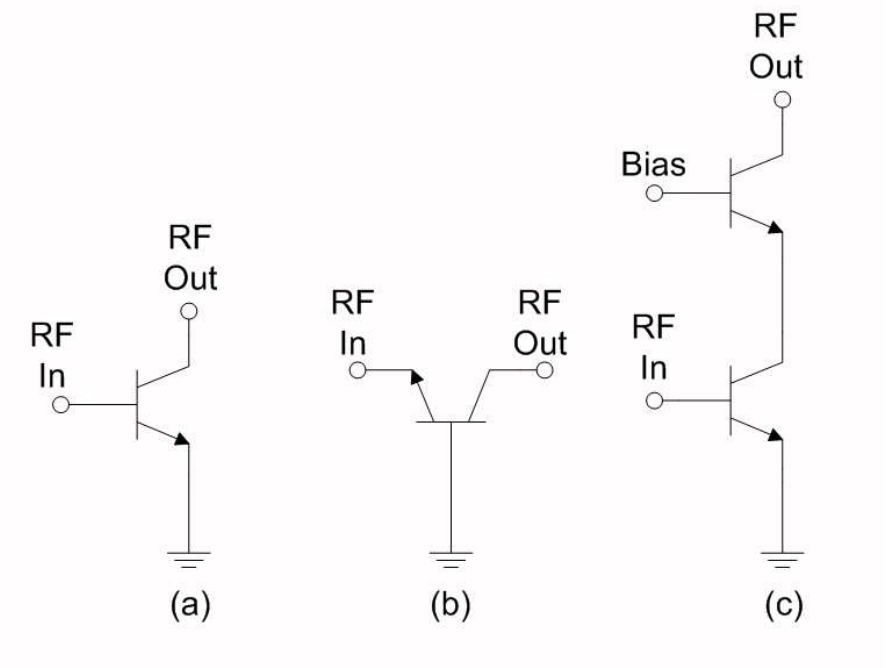

Figure 7: Configurations for (a) Common-Emitter (CE), (b) Common-Base (CB), and (c) cascode amplifiers.

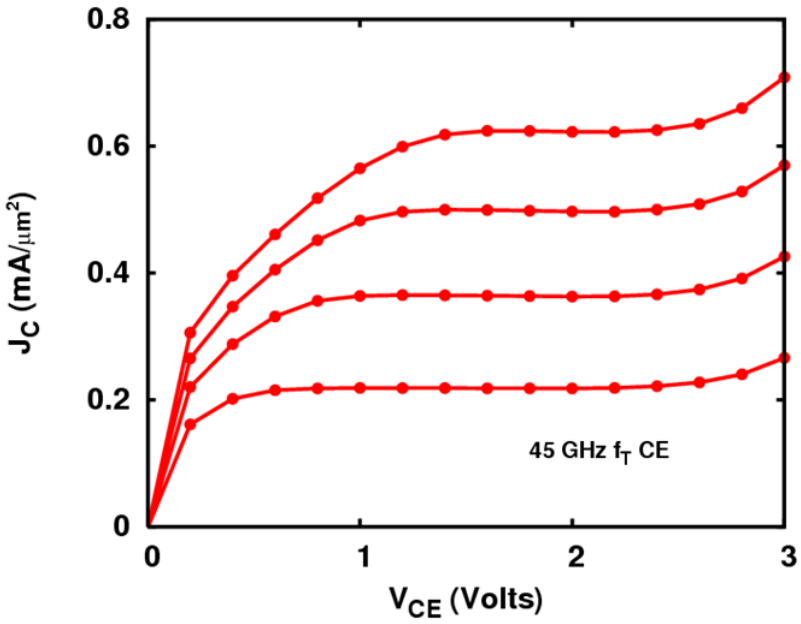

Figure 8: Output characteristic of a 45 GHz f_T device on J_C.

This correlates well with the BV_{CEO}, BV_{CBO} relationship shown in Figure 6. While the cascode configuration does exhibit an increased knee voltage since the voltage drop across the Collector-Emitter junction of the CE device is added in series with the CB device, the impact of this on PAE is related to the ratio of breakdown voltage to knee voltage, as shown in [37]. Since the breakdown voltage is greatly increased, it is possible to see increased PAE from the configuration. It is also noteworthy that the cascode acts to provide an improved linear operating range in the CB device, allowing for an increased peak current from a load-line standpoint [38].

2.3 Cascode Power Amplifiers

The ability to employ mixed breakdown voltage devices in the cascode allows for exploitation of the inherent values of each transistor. Using a higher breakdown, lower gain device in the CB portion of the cascode allows for increased operating voltages, as was shown in the prior section. Using a lower breakdown, higher gain device for the CE portion allows for greater gain, as is shown in Figure 10. The CE device is biased at nearly 0 Volts V_{CB} so as to minimize quiescent power dissipation while preserving the gain of the device.

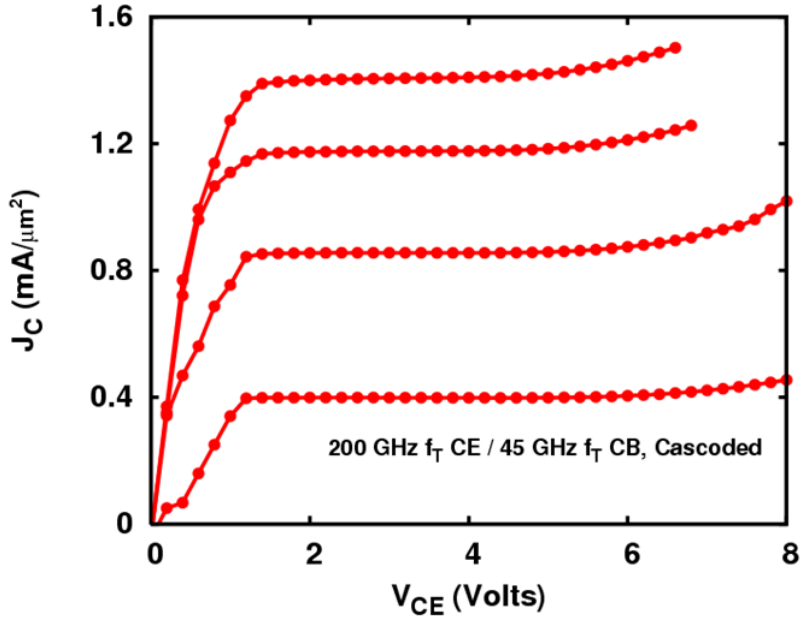

Figure 9: Output characteristic of a 200 GHz f_T CE device cascoded with a 45 GHz f_T CB device on J_C.

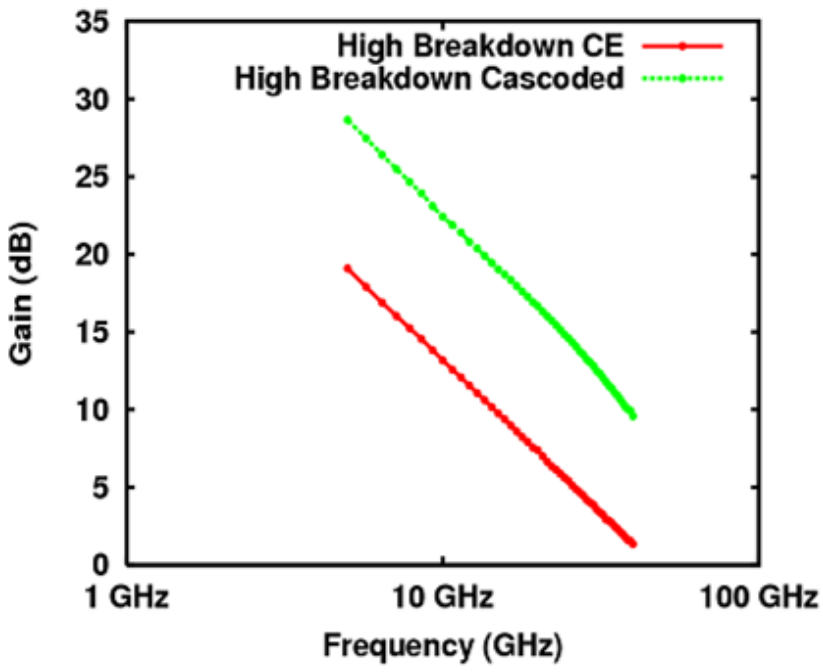

Figure 10: H_{21} gain of 45 GHz f_T CE device compared to the same 45 GHz f_T device in a CB configuration cascoded with a 200 GHz f_T device in a CE configuration.

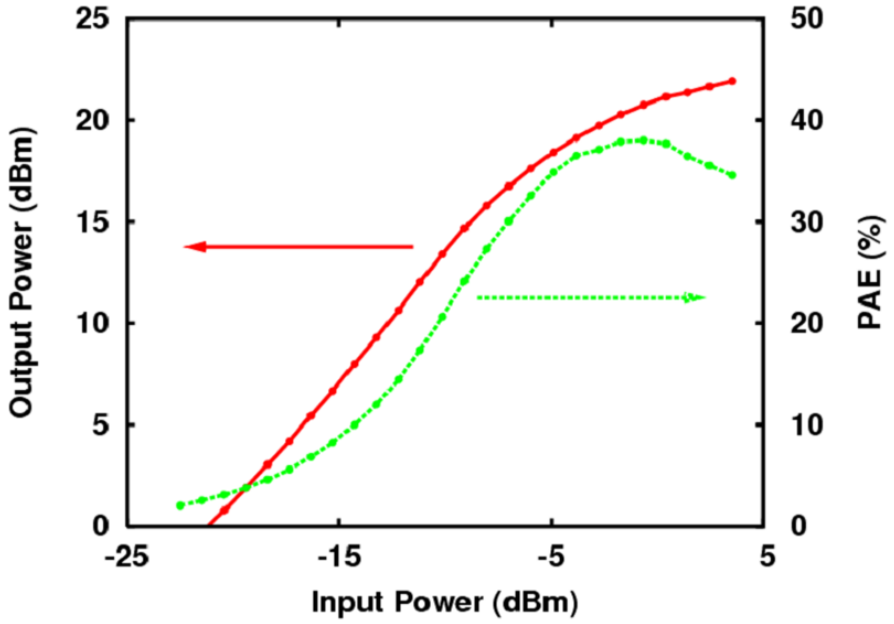

Figure 11: P_{out} and PAE of a power cell of 12 0.6x18 μm^2, 45 GHz f_T devices cascoded with 12 0.12x18 μm^2, 200 GHz f_T devices at 9.5 GHz.

A power cell, consisting of 12 devices with a peak f_T of 45 GHz and dimensions of 0.6x18 μm^2 as the CB device cascoded with 12 devices with a peak f_T of 200 GHz and dimensions of 0.12x18 μm^2 as the CE device, was fabricated and tested in a third generation SiGe technology. Load pull matched power output and PAE of the cell operated at 9.5 GHz is shown in Figure 11. In Class AB operation the cell exhibited 20.7 dBm of output power with a gain of 19.7 dB at a peak PAE of 38%. The cell was biased at a collector voltage of 5 Volts.

2.4 Summary

Increased breakdown voltages in SiGe for power amplifier applications are demonstrated through the use of forced emitter current and the Common Base amplifier incorporated in the cascode configuration. The use of a high-speed HBT in the CE portion of the cascode and a high-breakdown HBT in the CB portion allows for optimal performance of the amplifier for both gain and breakdown voltage. Increased available breakdown voltage and peak operating current have been shown. Results of the fabricated power cell show

excellent PAE and gain at moderate output power. The hybrid breakdown voltage cascode configuration shown here shows promise for higher output powers for power amplifiers at X-band and beyond.

CHAPTER III

A TWO-STAGE HIGH-GAIN POWER AMPLIFIER

3.1 Introduction

Utilizing the mixed breakdown cascode architecture, an HB/HS cascode is used to demonstrate a high gain, two stage power amplifier in a third-generation SiGe technology. Through the use of on chip biasing and matching, the amplifier is well-matched to 50 Ω input and output impedances, exhibits greater than 20 dBm of output power, 25% power-added efficiency (PAE) and 40 dB of stable power gain from 8.5 to 10.5 GHz (X-Band).

3.2 Breakdown Voltage in SiGe Devices

It is commonly accepted that low breakdown voltage transistor technologies are incompatible with efficient power amplifier design. Power amplifiers, unlike small-signal amplifiers such as LNAs, are not conjugately matched on their outputs, but instead are intentionally mismatched to drive a given output power. The optimal output power for a given power amplifier is derived from its maximum deliverable voltage and current, which also sets the load for the amplifier [38]. Consequently, the output load resistance of a power amplifier is related to the maximum breakdown voltage of its requisite transistors and the desired deliverable power by the well-known relation, $R = V^2/P$. Thus, the load line value for an amplifier increases as the square of the available breakdown voltage of the requisite transistors. The increased load match allows for decreased losses in the matching circuitry, which improves gain, output power, and PA efficiency [39], the latter of which is quite significant.

While a Common-Emitter configured high-breakdown SiGe transistor in a 200 GHz technology exhibits a breakdown voltage of just over 3 Volts, as seen in Figure 8, the same transistor, when configured in a common-base configuration, exhibits a breakdown voltage of nearly 8 Volts, as shown in Figure 9. This phenomenon is achieved through the physical mechanism of base current reversal [40]. As opposed to current flowing into the base of the Common-Base transistor, as is generally the case, at higher collector voltages, current

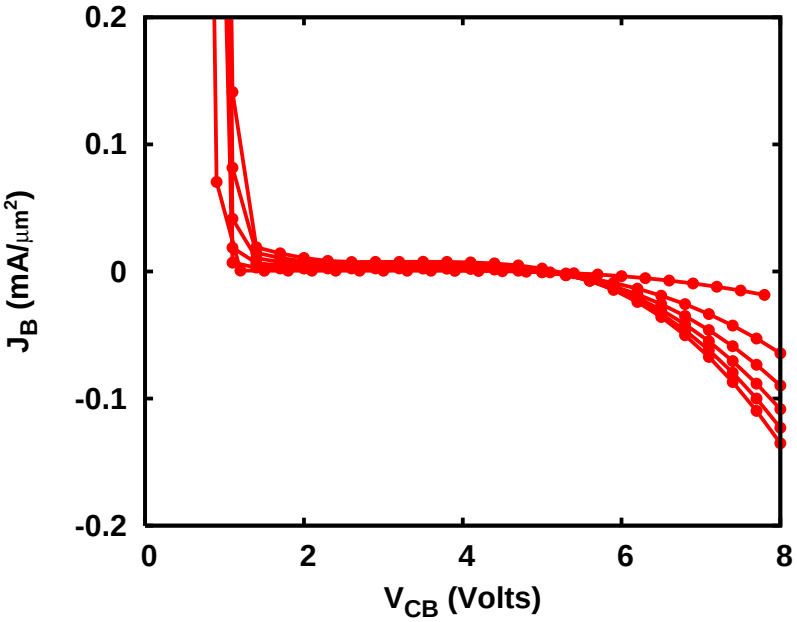

Figure 12: Base current flow in the high-breakdown, common base configured transistor of a cascode configuration, as a function of collector voltage.

actually flows out, since the base looks like a low impedance at DC. The base current reversal is explicitly shown in Figure 12. It is serendipitous that the bias point for the amplifier configuration occurs at a collector voltage below where the current reversal occurs. Thus, the bias circuitry need not sink any current, simplifying its design. It is necessary that ample capacitance be placed on the base of the high-breakdown device to provide the necessary current under RF drive conditions. This also coincides with the condition that the base appear as an RF ground, which is necessary to achieve the desired power gain and remain stable during operation.

3.3 Power Amplifier Design

The power amplifier was implemented in a commercially-available 200 GHz SiGe process technology. A schematic of the two-stage amplifier is shown in Figure 13.The first stage is made up of a single HS/HB pair of devices that are available in the design kit. The devices were sized such that, at optimal bias, each device operates near its peak f_T current.

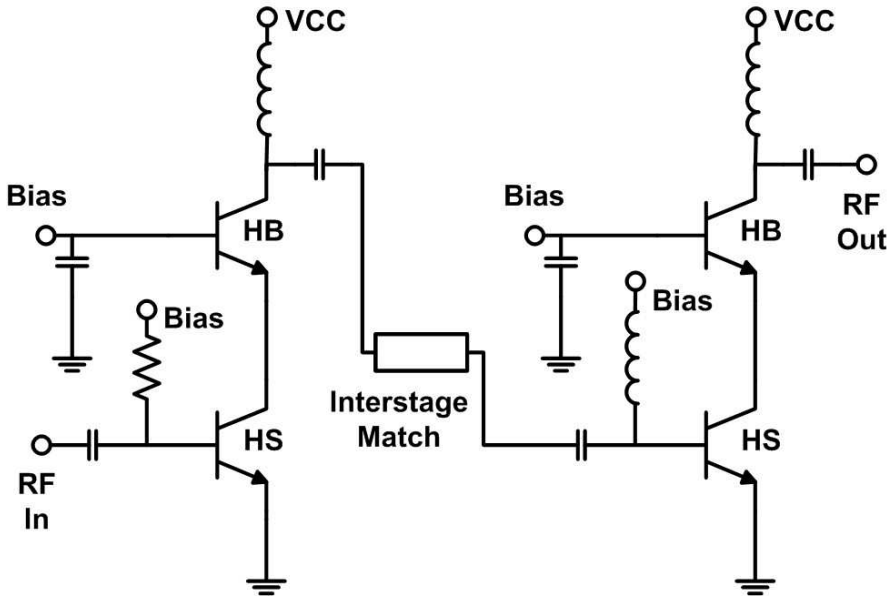

Figure 13: Schematic of the two-stage hybrid cascode power amplifier showing use of high-breakdown (HB) and high-speed (HS) SiGe transistors.

The ratio of peak f_T on J_C in this technology between the available high-speed and high-breakdown devices is nearly 8-to-1, making the emitter area of the HB device 8 times that of the HS device.

Using the maximum emitter geometry available for this particular SiGe technology would have required nearly 40 HB devices attached in parallel to meet the targeted output power for the second stage amplifier. This was deemed an unattractive choice from a real estate perspective, as well as adding unwanted interconnection parasitics. Consequently, a larger device with 5 times the area of the largest available HB device was designed and modeled for use in the second stage. Eight HS/HB pairs were then used to achieve the desired output power.

To match to the relatively small input impedance of the second stage, on-chip microstrip transmission lines fabricated in the top two thick (Al) metals available in the technology were employed. This was done out of necessity of a series inductive element, either pure or distributed, to match. Space requirements prohibited the use of available on-chip spiral inductors. The incorporation of both foundry provided models and EM modeling of corner joints and T-junctions was used to obtain the series contribution of the meandered

transmission line for fine-tuning the interstage match.

Large banks of lumped capacitance utilizing on-chip MIM (metal-insulator-metal) capacitors, on the order of 10 pF, were used at the base of the common-base transistor in each stage. Trace lengths between the transistors and the capacitors were kept symmetric and as short as possible to minimize series resistance and inductance.

To further ensure robust stability of the amplifier (given its large on-chip gain), layout stabilization techniques were also employed. The core layout of the amplifiers themselves kept the CE input base and the CB output collector of the cascode as far away from each other as physically possible. Isolation rings were placed around all inductors, which consisted of metal walls comprised of regularly spaced vias and routing metal which spans from the top metal layer down to the substrate. This was done to minimize the possible positive feedback from the output and interconnect stages into the inputs of earlier stages.

The designed operational frequency of the amplifier was 8.5 to 10.5 GHz to support the intended X-band radar application. Both input and output ports were matched to 50 Ω using available on-chip passives. An input bias resistor was used to save space compared to using an inductor on the first stage, and also to improve the broadband S_{11} performance. Post-extraction simulation results showed a worst case 41 dB of gain with an output power of 20.4 dBm across band, with a PAE of 31%.

3.4 Measured Results

The fabricated amplifier exhibited excellent input matching to 50 Ω across the entire operating frequency, as can be seen in Figure 14. The output power match for the second stage was also well-matched across the band to the 50 Ω system impedance, as shown by the 1 dB power contours in Figure 15 and the 3% PAE contours of Figure 16.

The input and output matching contributed directly to the measured output power meeting (and exceeding) the simulated performance at mid and high frequencies in the band of operation, as shown in Figure 17. The interstage match was slightly off in frequency, which accounts for a lack of drive power to the second stage, resulting in lower output power and PAE at the low end of the band. PAE at low, mid, and high ends of the band is shown

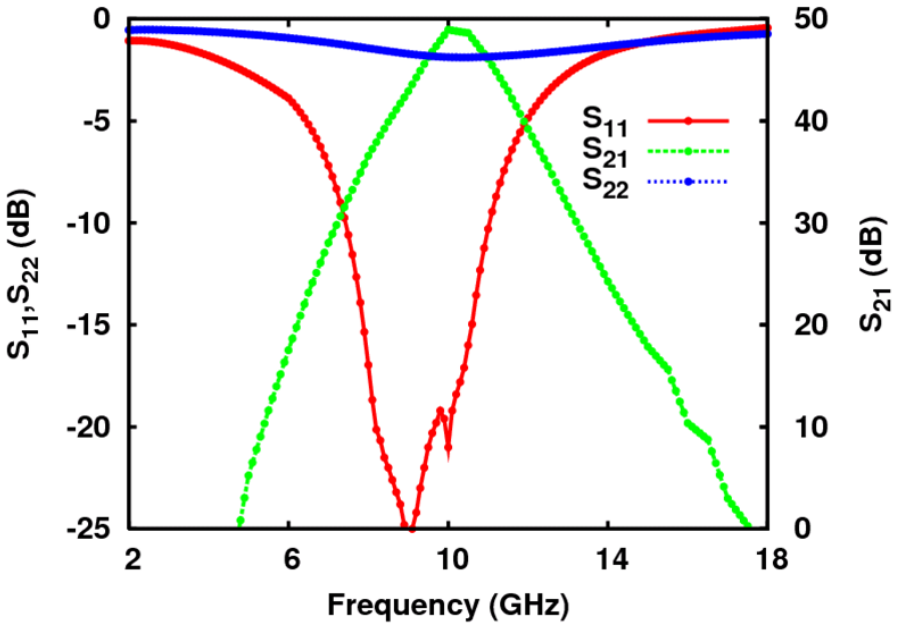

Figure 14: Measured S-parameters of the two-stage SiGe amplifier.

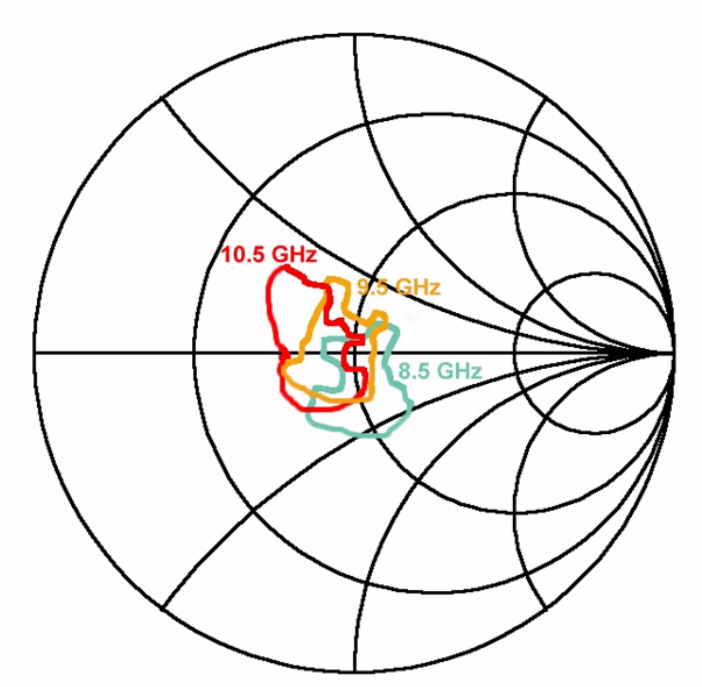

Figure 15: 1 dB power contours at low, mid, and high frequency points showing excellent match to 50 Ω.

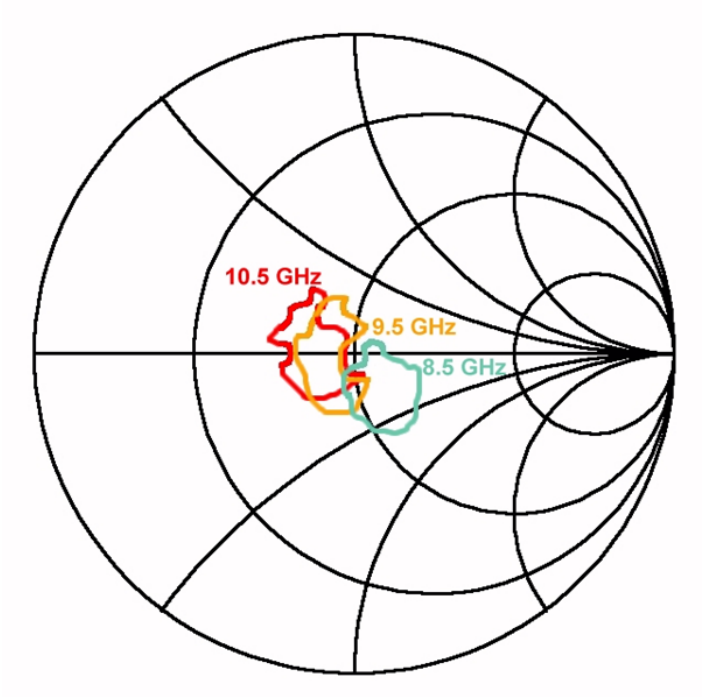

Figure 16: 3% PAE contours at low, mid, and high frequency points.

in Figure 18.

The output power and PAE are comparable to the SiGe power amplifier reported in [41] which is at a similar operational frequency. Through the use of the hybrid breakdown voltage cascode architecture employed here, a gain increase of nearly 20 dB was achieved over this previous result. In addition, using the non-optimized technique in [41] would require twice as many amplifier stages. Such a design would be significantly more difficult to design and be more susceptible to the instability and in-efficiency which often results when using more interstage matches.

3.5 Design Improvements

Following incorporation of the two stage amplifier into a full X-Band T/R module with accompanying LNAs and phase shifters, an out of band oscillation at 12 GHz was witnessed which could not be eliminated through external bypassing of the module. The poor low band performance of the amplifier also did not provide ample margin to reach module system level goals. Consequently, minor design changes were made to the amplifier.

Simultaneous large signal and high gain operation, as is the case with the mixed cascode

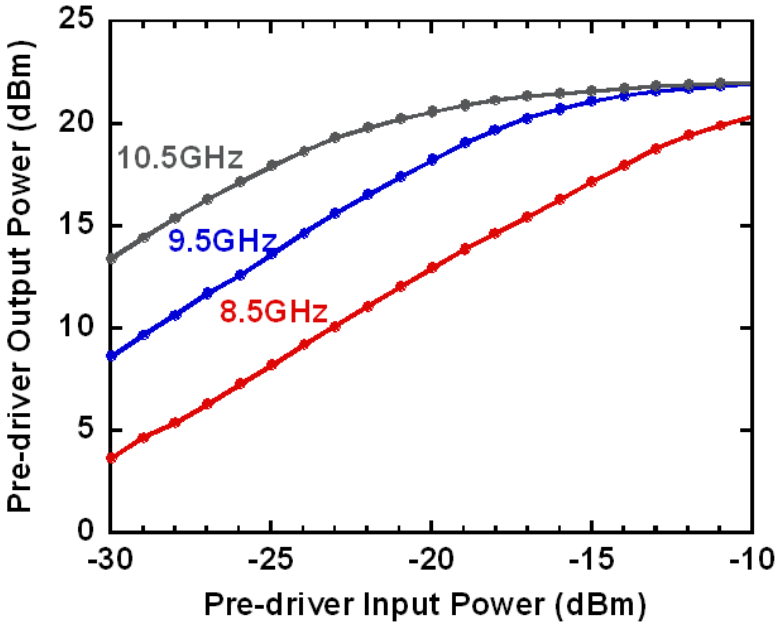

Figure 17: Output power as a function of input power.

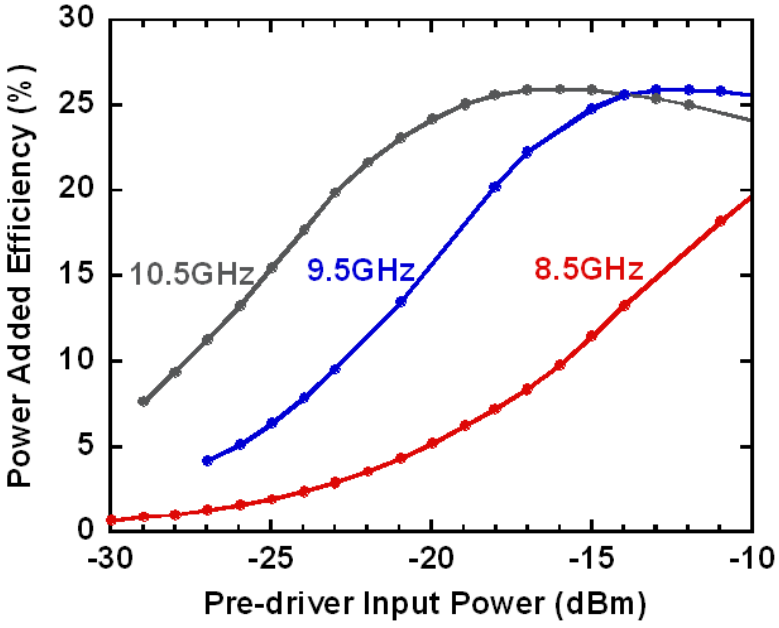

Figure 18: Power Added Efficiency as a function of input power at low, mid, and high frequencies.

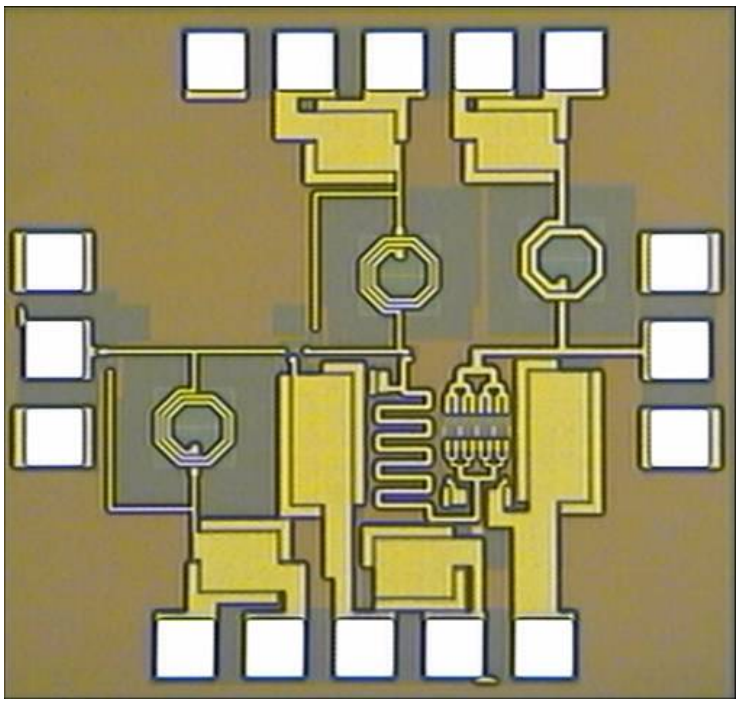

Figure 19: Die photo of the two-stage SiGe amplifier, measuring 1.1 mm x 1.2 mm in area, including pads. Some of the discernible features include the on-chip spiral inductor feeds, large banks of MIM capacitors, and microstrip transmission line matching elements.

amplifier, has the ability to become unstable, especially at lower, out of band frequencies where even higher gain than the in-band gain is experienced. Proper capacitive bypassing on and off chip is crucial, as is focusing on interstage impedance matching in and out of band. Points of improvement for the two stage power amplifier were: 1) interstage match between the two stages, 2) appropriate bypassing and bias feed network for the upper base in the mixed cascode, and 3) appropriate bypassing on collector supply.

Further s-parameter analysis of the interstage match demonstrated not only that it was slightly mis-tuned for gain, but that it also had a potential instability through the translated impedance of the first stage output to the second stage input. Minor modifications to the length and coupling of this line remedied this problem. A slightly different interstage issue was the interconnect between the high and low breakdown devices in the mixed breakdown cascode. As has been previously mentioned, it is critical to make the upper base of the cascode look as close to AC ground as possible. Unfortunately, layout limitations within the original design predicated that the connection to the upper base be longer, and consequently

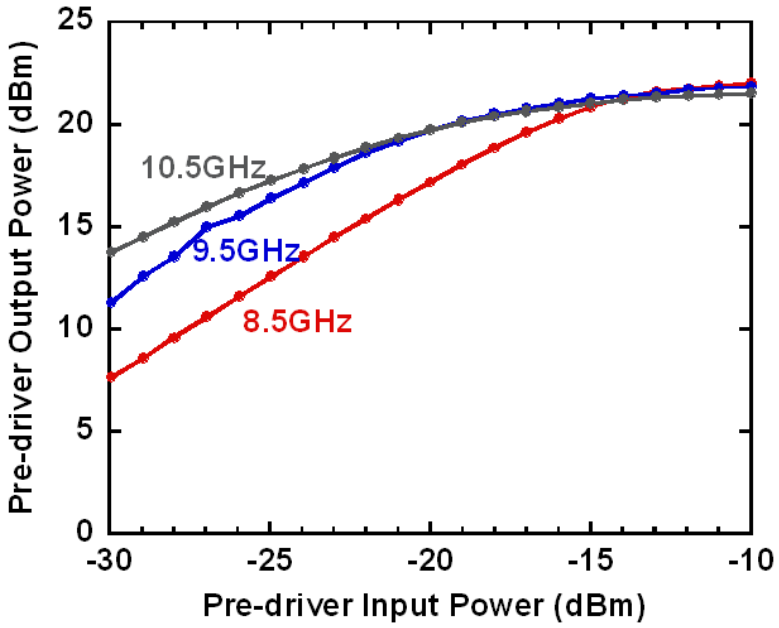

Figure 20: Output power after design modifications.

more inductive, than was tolerable by the design. This was done in an attempt to achieve symmetry and keep all phases equal. Focusing the layout on minimal upper base trace length and ignoring phase issues resulted in a much lower base inductance and drastically improved stability. Finally, additional capacitance was added to both the upper base and collectors on chip to provide more rejection to oscillations.

The resultant amplifier showed no oscillatory behavior when incorporated into the T/R module and measured at the chip level. Additionally, the power and power added efficiency achieved at the low end of the band were greatly improved, as is seen in Figure 20 and Figure 21. This increase in output power and efficiency was sufficient to achieve chip level system goals. Comparable power amplifiers in multiple different mm-wave processes are shown in Table 2. This amplifier competes favorably in both output power and efficiency, especially given the available breakdown voltage in the process. It also represents the highest gain per stage of a power amplifier at X-Band, to the best of the author's knowledge.

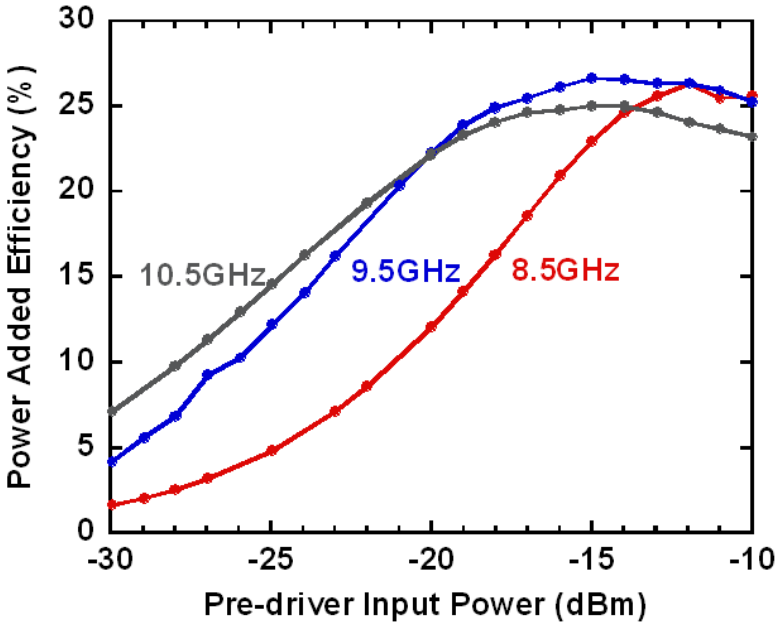

Figure 21: Power Added Efficiency after design modifications.

Table 2: High Gain X-Band Power Amplifiers.

Process	**Stages**	**Output Power (dBm)**	**Gain (dB)**	**PAE (%)**	**Breakdown Voltage (Volts)**	**Frequency (GHz)**	**Ref.**
SiGe	2	25	24	35	5	7-11	[41]
SiGe	1	17.5	15	10.1	2.4	7-18	[42]
CMOS	1	19	8.2	25	-	3.7-8.8	[43]
CMOS	2	23.5	29	19	3.3	8.5-10	[44]
CMOS	1	3.5	17	2.2	2	2-8	[45]
GaAs	1	24.2	8.3	35	9	12.2	[46]
SiGe	2	23	40	25	3.3	8.5-10.5	This Work

3.6 T/R Module Integration

The two stage stand-alone power amplifier was integrated with a 4-bit phase shifter, two LNAs, and assorted switches to realize a functional X-Band T/R module that operates from 8.5 GHz to 10.5 GHz. The block diagram of the amplifier is shown in Figure 22. The phase shifter is common to both transmit and receive paths. A Single Pole Double Throw (SPDT) switch at the manifold of the module selects between transmit and receive. System requirements called for two possible receive paths, so a Single Pole Triple Throw (SP3T) switch at the output actuates between two LNAs and the two stage power amplifier. A circulator, external to the chip, combines the three outputs to a single antenna. The two LNAs receive from opposite polarities on the antenna [3].

The T/R module was realized in an area on chip, including bond pads, of 3.5 mm x 3.8 mm, as is shown in Figure 23. The phase shifter occupies the majority of the on chip real estate, with the power amplifier and two LNAs occupying a similar area of around 1 mm^2.

Mid band output power is shown in Figure 24 and mid band gain and PAE are shown in Figure 25. The output power is nearly identical to that of the stand alone amplifier, since the outputs of the two configurations are the same. The PAE is slightly lower, since the overall transmit gain is greatly reduced by the presence of the phase shifter and assorted in-line switches.

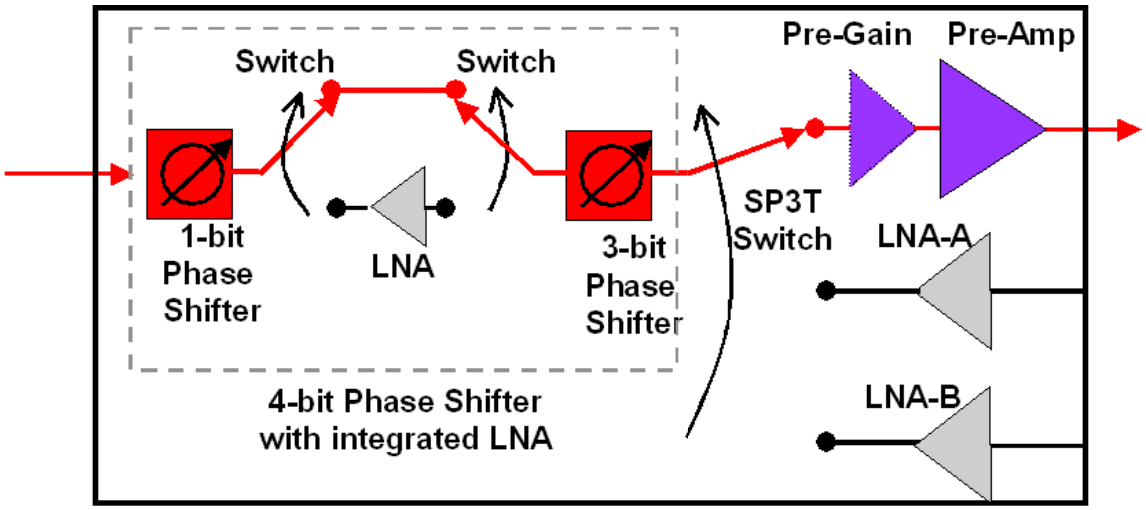

Figure 22: Block Diagram of X-Band T/R module showing 4-bit phase shifter, two LNAs, both stages of the mixed cascode power amplifier (labeled as Pre-Gain and Pre-Amp), and assorted switches.

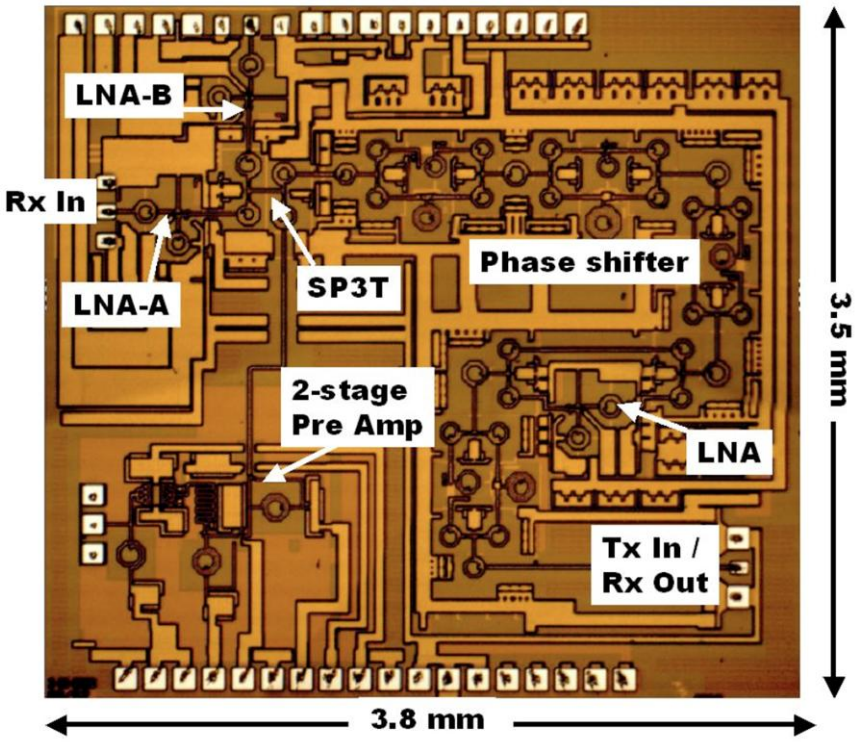

Figure 23: Die photo of the integrated T/R module on SiGe.

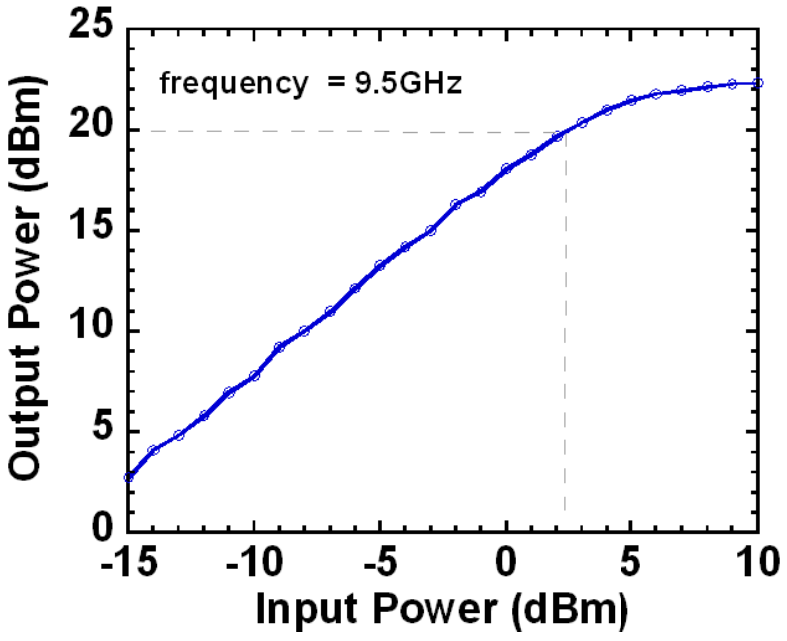

Figure 24: Measured output power of integrated T/R module.

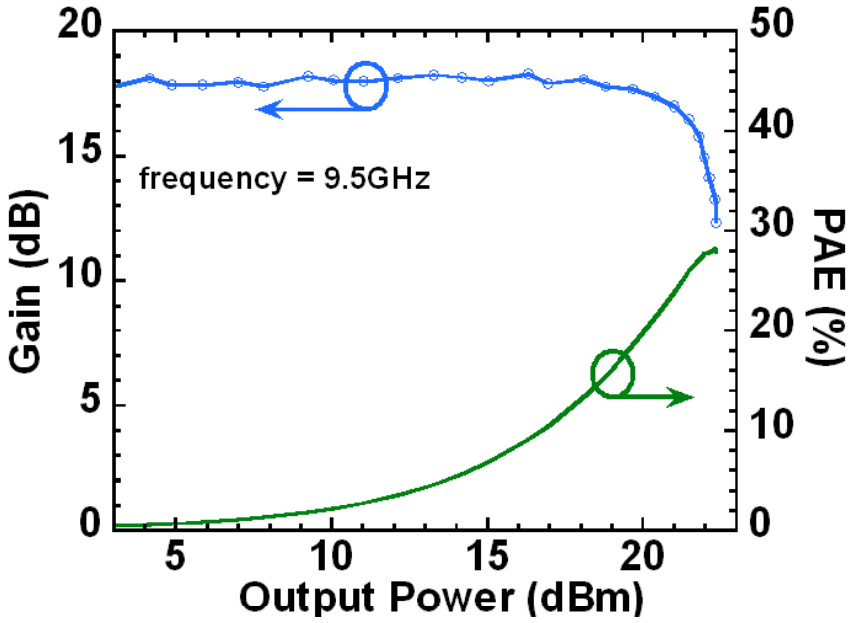

Figure 25: Gain and efficiency of the T/R module's transmit path. Lower gain is a symptom of greater than 20 dB of loss through the phase shifter and switches.

3.7 Summary

SiGe continues to show that it is a viable contender for many microwave circuit applications. An optimal use of hybrid high-breakdown and high-speed devices available in SiGe technologies, when combined in the cascode topology, can provide excellent gain and high voltage swing (efficiency) for SiGe power amplifiers. The fabricated two-stage SiGe power amplifier exhibits greater than 40 dB of gain with an output power of greater than 20 dBm and a PAE of greater than 25% at X-Band. Use of the hybrid breakdown cascode topology in SiGe is demonstrated to be a powerful technique for reducing the number of amplifier stages needed to obtain the desired overall gain, while simultaneously improving matching through increased breakdown voltage. This two-stage amplifier was successfully integrated into an X-Band T/R module operating from 8.5 to 10.5 GHz.

CHAPTER IV

A NEAR ONE WATT SIGE POWER AMPLIFIER

4.1 Introduction

Utilizing the mixed breakdown cascode architecture presented in [1], a SiGe power amplifier capable of producing 850 mW has been developed. The device is matched to 50 Ω at the source and has four separate output stages, which when combined off-chip provide a CW output power of 850 mW at 9.5 GHz with 11 dB of gain and a PAE of 18%. To the authors' knowledge, this result represents the highest output power achieved to date in SiGe at X-Band frequencies.

4.2 Power Amplifier Design

The power amplifier was implemented in a commercially available, third generation, 200 GHz SiGe BiCMOS process technology. The mixed cascode power amplifier core consists of four sub-amplifiers of identical design which were combined to a single input nominally designed to be 50 Ω. Each of the four sub-amplifier's outputs was left uncombined and unmatched on-chip. Both simulation and test of on-chip passives showed that they were incapable of handling the power necessary at the output and contributed to excessive loss. The standard low pass configuration of inductance through bondwires and shunt capacitance using off-chip, high-quality single layer capacitors, is ultimately employed in the final amplifier design.

Each sub-amplifier is comprised of 32 HS/HB cascode core devices. Each of these devices employs a dedicated 0.6 μm x 20 μm emitter area HB device with a 0.12 μm x 20 μm emitter area HS device. The ratio of J_C needed to reach peak f_T between the HS and HB devices in this SiGe process is nearly 8:1, and since the two devices share a common collector current, the ratio of emitter areas should be on this order. The ultimate ratio of 5:1 was determined through simulation to provide the best HS collector to HB emitter matching. To minimize losses on the output while preserving routing path length, a binary combination

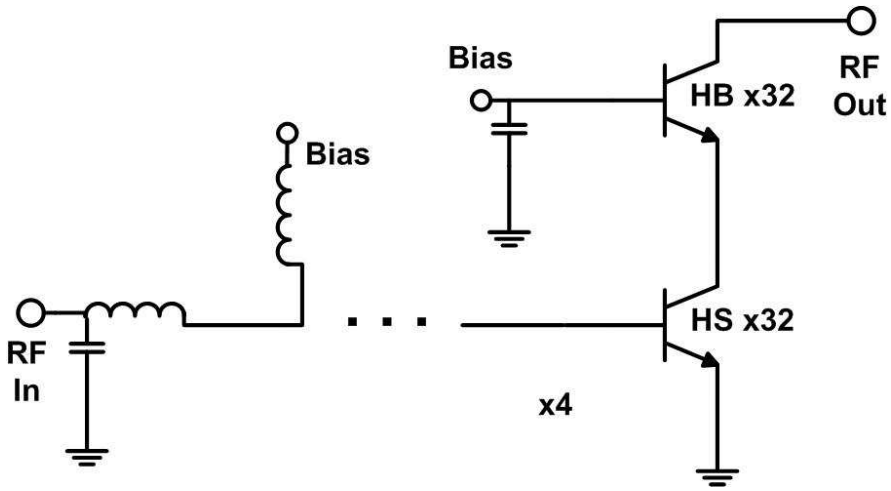

Figure 26: Schematic of the hybrid cascode power amplifier showing matching elements and use of High-Breakdown (HB) and High-Speed (HS) SiGe transistors.

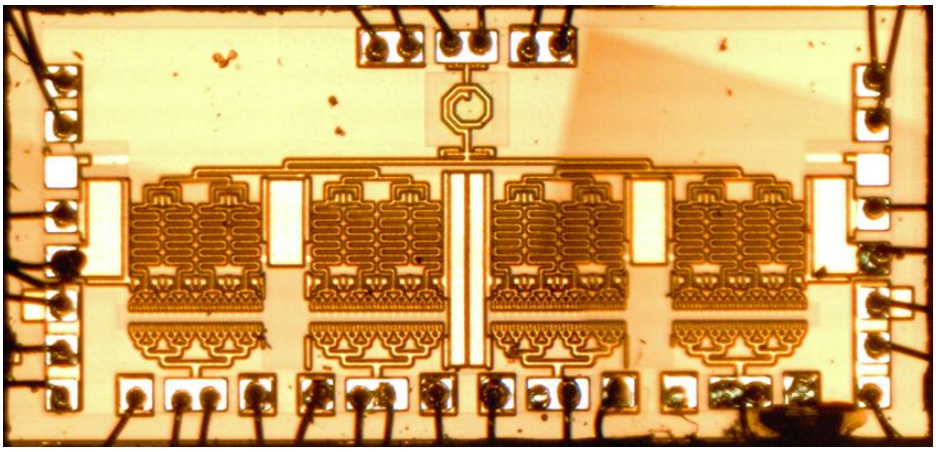

Figure 27: Die photo showing input matching sections consisting of a spiral inductor and meandered microstrip transmission lines. The output combining network of the four parallel stages can also be seen. The overall die size, including pads, is 1.5 mm x 3 mm.

tree structure was used to combine the HB collectors. The input devices were periodically matched to higher impedances through series-meandered microstrip transmission lines and shunt MIM capacitors available in the process. The inputs of the four sub-amplifiers were then ultimately combined into a single feed and matched to 50 Ω through a final spiral inductor and shunt MIM capacitor at the input. A schematic of the amplifier is shown in Figure 26.

Each core layout was parasitically extracted and combined on the input and output with microstrip transmission lines fabricated with the upper, thick layers of aluminum available in the SiGe Back End Of the Line (BEOL) process to minimize ohmic loss. Harmonic balance simulations of the sub-amplifiers showed a 1 dB compressed output power of 26.6 dBm with 11 dB of gain and a PAE of nearly 28% at the mid-band frequency of 9.5 GHz, with an output impedance of $8 - j6$ Ω. A die photo of the fabricated amplifier is shown in Figure 27.

4.3 Measurement Setup

The SiGe die were epoxied down and bonded out to a printed circuit board consisting of 25 mil thick Rogers 3010 material with a dielectric constant of 10.2. The pad to which the base of the SiGe was attached was heat sunk to the backside of the wafer through many thermal vias and then ultimately to the chuck through contact with the backside. The input was bonded directly to a 50 Ω transmission line which had been fabricated on the Rogers material. The outputs were bonded to a power combiner which ultimately terminated in a 50 Ω transmission line. High Q, discrete, X-Band capacitors to ground were placed one quarter wave away from the output and input 50 Ω transmission lines for stability purposes over frequency. Additional lower frequency, discrete bypass capacitors were also placed on the input, output, and upper base inputs on the Rogers material to assist in low frequency stability.

TRL standards on the Rogers material were used to set the measurement reference planes at both the bondwire terminations on the input 50 Ω line and at the 50 Ω combination of the four power outputs. A Maury load pull system, calibrated to these planes, was used for

both load and source pull measurements of the die. The Momentum EM solver available in Agilent ADS was used to simulate the phase and loss in the power combiner and to transform the measured combined output back to that of the individual outputs at the combiner plane. Utilizing the bondwire model in [47] and measured parameters on the bondwires used, the effect of the output bondwires were deembedded and the impedances were transformed back to the pads on the output of the die.

To verify stability, the largest available VSWR circle afforded by the loss in the tuners at the calibration frequencies was swept on the input and on the output, which was slightly in excess of 10:1. No oscillations were exhibited during the VSWR tests.

4.4 Load Pull Results

The amplifiers were driven in a constant current drive, Class A mode of operation. While each core was designed to handle nearly 500 mA of bias current, diminishing returns on PAE vs. increased power were experienced at bias levels much above 250 mA per core. Consequently, lower bias currents than were designed for were used. The use of lower collector current results in improved output impedances at the four sub-amplifier outputs by reducing the slope of the load line.

The input impedances, being small-signal in nature, are relatively independent of the change in bias point. The measured values at low, mid, and high band across the designed operating frequency of 8.5 GHz to 10.5 GHz are shown in Figure 28. The nominal impedance at 9.5 GHz was real in nature, but fell short of the 50 Ω design point and was instead closer to 40 Ω. The imaginary component of the input impedance was well-captured by simulation with the resultant impedances falling within the 1.8 VSWR circle shown, resulting in better than -11 dB return loss across the band.

As is shown in Figure 29, the real component of the measured output of the sub-amplifiers is nearly 14 Ω, which will allow for improved bandwidth in the subsequent off-chip output matching stage. The mid-band gain and output power are shown in Figure 30, with the designed-for gain of 11 dB achieved at the 2 dB compression point. Combining the output power of the four stages results in 29.3 dBm, nearly 850 mW, with an 18% PAE.

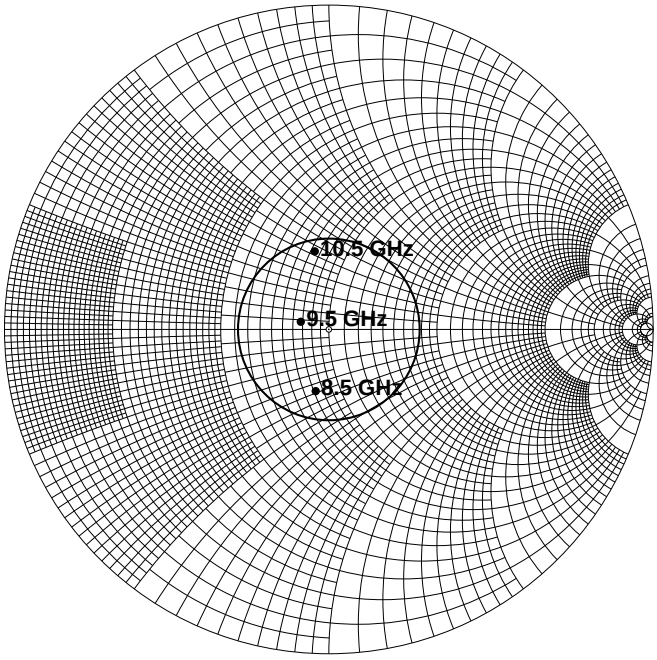

Figure 28: Source impedances at low, mid, and high band with a VSWR circle of 1.8 which correlates to a worst case return loss of -11 dB.

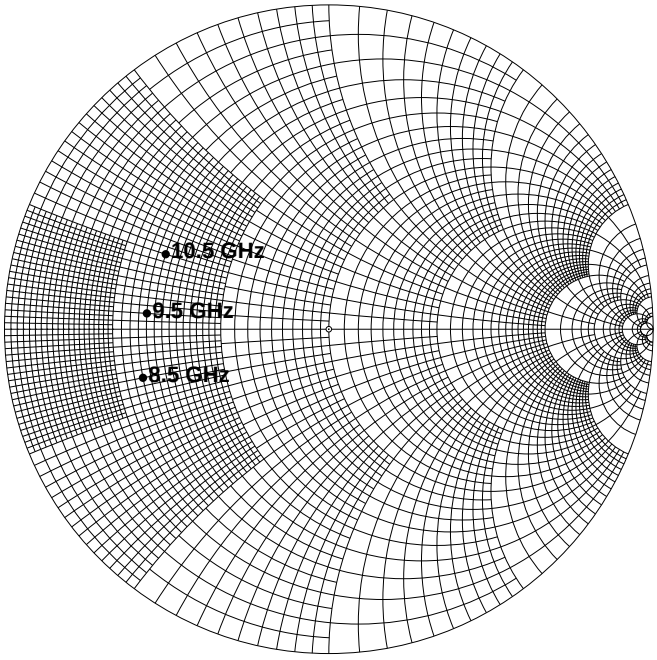

Figure 29: Output impedance of each of the four sub-amplifier output stages at low, mid, and high band.

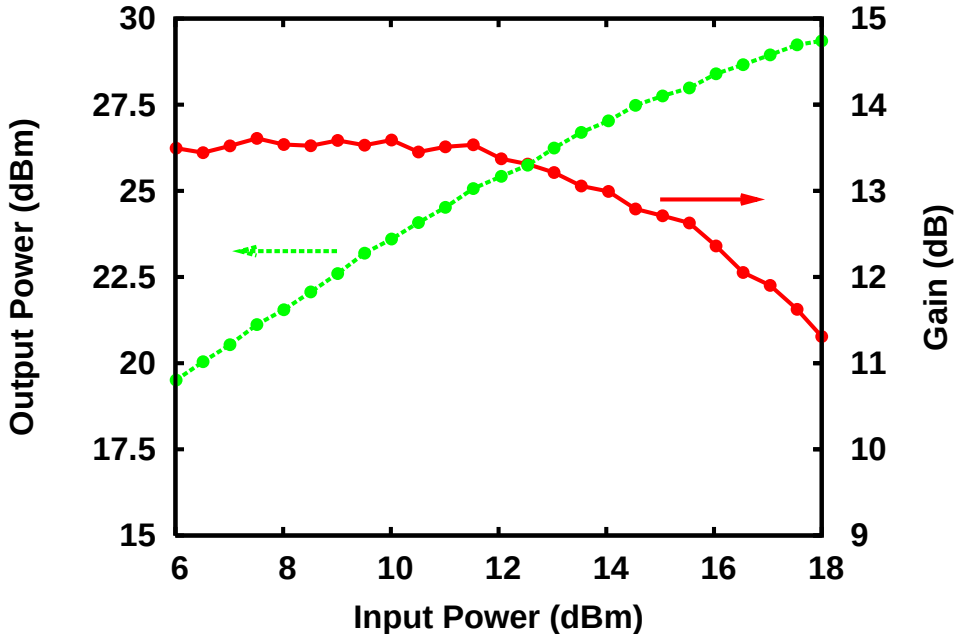

Figure 30: Output power and gain at 9.5 GHz for matched output condition referenced back to output pads on the die.

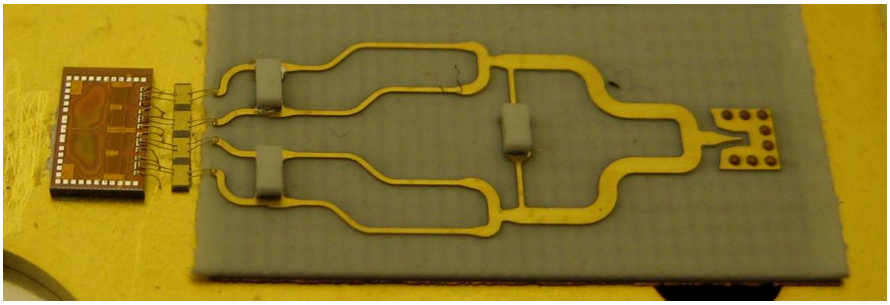

Figure 31: Power amplifier realization through off chip matching and power combining.

4.5 Output Power Combiner

Leveraging the load pull results from the previous section, an output combining network for the PA was designed to achieve a working power amplifier with a single input and output port. This was achieved by using the inductance of the output bond wire, high quality off-chip single layer capacitors, and a multi-section Wilkinson power combiner fabricated on a circuit board material. The ultimate configuration is shown in Figure 31.

As opposed to the previous experiment, the die was not epoxied down to the board material, but instead, the die, single layer capacitors, and printed circuit board were all

epoxied down to a gold plated molybdenum-copper heat spreader. This was done for two main reasons. First of all, the gold surface of the heat spreader serves as the ground for the entire circuit and realizes a configuration with minimum emitter inductance seen by the power amplifier. The previous configuration had to go through ground vias in the board material which increased both the ground inductance and the potential for oscillatory behavior. Secondly, molybdenum-copper alloy is an excellent heat spreader material and was used in an attempt to remove as much heat as possible away from the die. The single layer bar capacitors used were off-the-shelf components which are similar in structure, value, and quality (Q) to on-chip metal-insulator-metal capacitors. The Wilkinson power combiner was fabricated on a lower dielectric constant material, Rogers 4350, than the prior experiment, to allow for the realization of 50 Ω lines on a thinner substrate to allow for shorter bond wires from the single layer capacitors to the circuit board.

It was still possible to drive the input from ground-signal-ground (GSG) chip probes since the input was matched on chip. The Wilkinson power combiner was designed such that the microstrip transitioned to a coplanar waveguide and was also probable with on-wafer GSG probes. Measured results at the mid-band frequency of 9.5 GHz showed an output power in excess of 28 dBm and a PAE of 11%, further validating the load pull results on the individual cells. The output match was near 50 Ω, as can be seen in Figure 32. While minor changes in the output combining network could improve the output impedance, further testing needs to be employed with a lower noise driver amplifier. The Traveling Wave Tube (TWT) amplifier used exhibited a very high noise floor, which acted to saturate the amplifier under test conditions and did not allow it to reach its peak output power or load impedance. A better driver amplifier should allow for a measured increase in output power, PAE, and potentially load impedance. Comparable output power amplifiers in SiGe and GaAs are shown in Table 3. While the presented amplifier is low in PAE, it should be noted that it represents the lowest breakdown voltage process of all competing amplifiers.

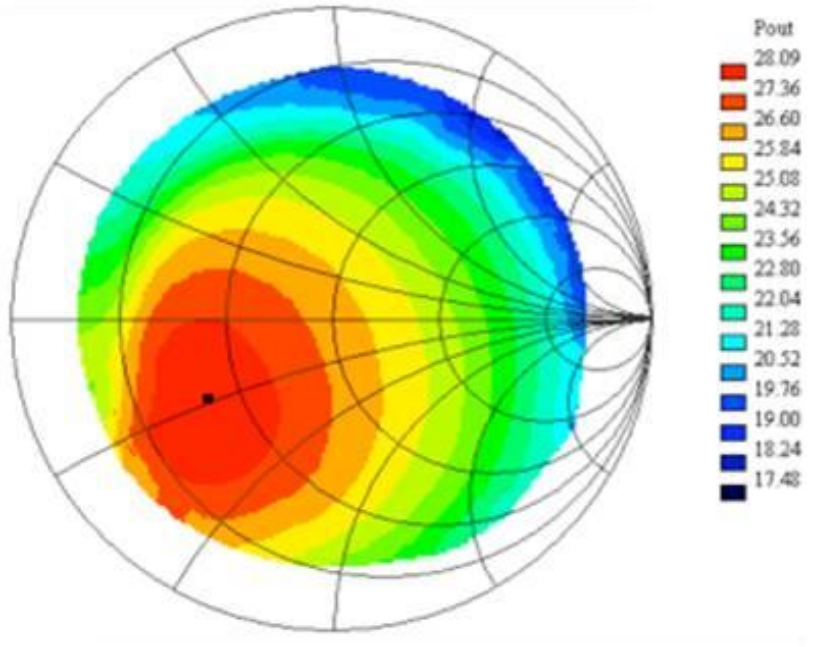

Figure 32: Load pull results at 9.5 GHz for the power amplifier in Figure 31.

Table 3: X-Band Power Amplifiers with near 1 Watt performance.

Process	**Output Power (dBm)**	**Gain (dB)**	**PAE (%)**	**Breakdown Voltage (Volts)**	**Frequency (GHz)**	**Ref.**
SiGe	24.8	8.6	28	7	8.4	[48]
SiGe	25	24	35	5	7-11	[41]
GaAs	36.3	18	25	7	9-11	[49]
GaAs	26	16	26	7	9-12	[50]
GaAs	37	9	35	8	9-10.5	[51]
SiGe	29.3	10	19	3.3	9.5	This Work

4.6 Summary

A SiGe power amplifier with an output power of 850 mW at X-Band frequencies and a single stage gain in excess of 10 dB is presented. Although SiGe as a technology has very low breakdown voltages compared to competing III-V technologies, through use of the mixed breakdown voltage cascode topology, these breakdown voltages have effectively been more than doubled. Four sub-amplifiers, each consisting of 32 HS/HB cascode pairs were combined to a 50 Ω input impedance with the combined power of the amplifier at the die output achieving 29.3 dBm of output power. To the authors' knowledge, this represents the highest output power at X-Band in SiGe in the literature. This SiGe amplifier fulfills the single missing component, high-output power PAs, that are necessary for realizing complete X-Band systems in a SiGe platform.

CHAPTER V

THERMAL COUPLING ANALYSIS

5.1 Introduction

Thermal interactions between emitter fingers in a transistor and between fingers in adjacent transistors can drastically, and many times catastrophically, affect the electrical performance of devices. Electro-thermal feedback intra- and inter-device has been studied extensively on III-V [52][53] devices as well as Silicon On Insulator (SOI) [54][55], where relatively poor thermal conductivities make emitter finger spacing a significant issue. Due to the high thermal conductivity of silicon, most thermal interaction studies in SiGe HBTs have been limited to multi-finger single transistors [56].

As the performance of SiGe increases to beyond the 500 GHz peak f_T mark [26], so increases device finger power density. Increased speed results in lower breakdown voltages, but higher current densities, with the latter increasing more rapidly than the former is decreasing. This increasing BV_{CEO}, J_C product, shown in Figure 33 is directly proportional to an increased device temperature. Such increasing temperatures can cause similar inter-device thermal effects as those seen in other technologies. In addition, minimum spacing rules used in current IC designs allow for spacings between devices which can be smaller than the effective length of the device itself, which compromises the ability to accept the mutual thermal coupling factor R_{21} as a lumped element.

One-dimensional thermal layout techniques in SiGe as they apply to power amplifiers have been studied [57]. Thermal effects of minimum spaced transistors at various layout orientations in SiGe are analyzed. Through the use of infrared photography, heat across a device under test caused by an adjacent device which is running at a much higher temperature is measured. This demonstrates varied temperature gradients across active fingers as a function of orientation, correlates this to an effective operating temperature, and reveals the effects that this causes on operation of the measured device.

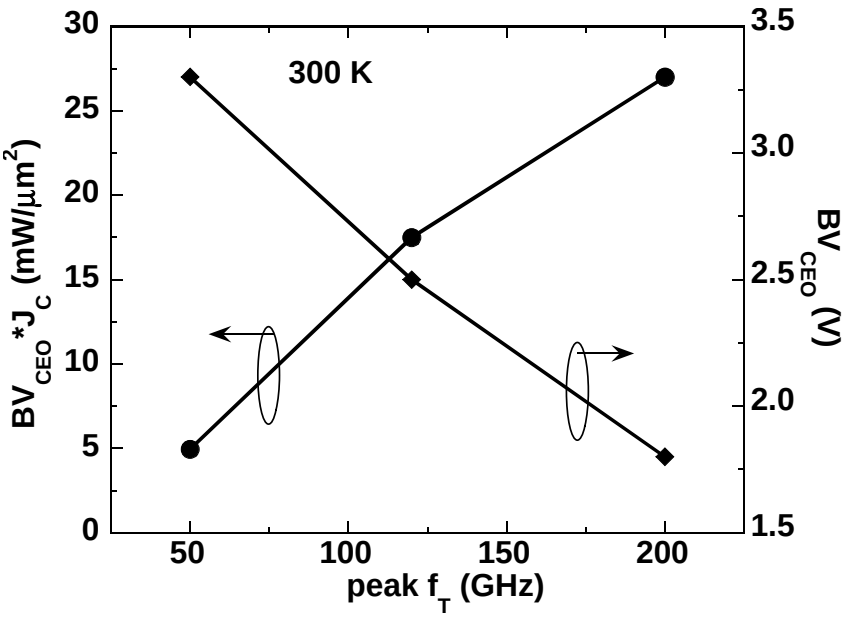

Figure 33: Breakdown Voltage, Current Density product vs. peak f_T in SiGe device technologies.

5.2 Thermal Coupling

From the definition of collector current in an HBT, which is given as

$$I_C = I_S \exp \frac{V_{BE}}{\frac{kT}{q}} \tag{10}$$

it is clearly seen that there is an inverse relationship between base-emitter voltage and temperature. The base-emitter voltage temperature coefficient is defined as

$$\varphi = \left. \frac{\partial V_{BE}}{\partial T} \right|_{I_C} \tag{11}$$

and is furthermore shown to be a temperature independent constant for a given value of I_C, as is shown in [58]. A base-emitter voltage change from an ambient voltage V_{BE0}, which corresponds to an ambient temperature T_0, can be used to calculate a corresponding temperature change and, ultimately, the operating temperature of a given device as

$$T_1 = -\frac{V_{EB1} - V_{EB0}}{\varphi} + T_0 \tag{12}$$

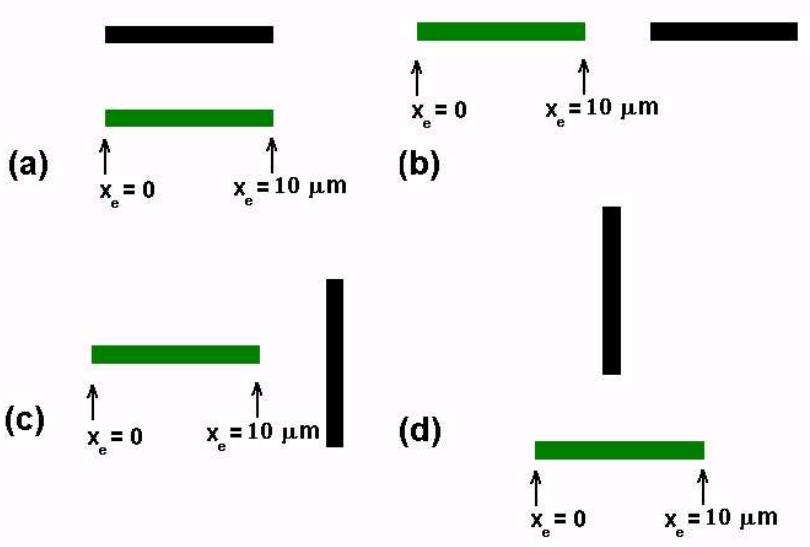

Figure 34: Four measured transistor orientations with measured device shown in green and heat source device shown in black. In subsequent plots, these orientations will be referred to as a) | |, b) − −, c) − |, d) | −, where the left device is the measured one.

5.3 Experiment

Using a 50 GHz SiGe process, 0.6 x 10 μm^2 single emitter devices were fabricated in a common-base configuration in the four orientations shown in Figure 34. For cases a) and b), minimum spacing of 4 μm between devices, as well as 10 μm were designed. For the cases of c) and d), only the 10 μm space was available.

Thermal images were obtained of the devices under operation through use of a Quantum Instruments Infrascope II thermal imaging camera. An example image is shown in Figure 35. This camera has a thermal resolution equal to 2 μm. To obtain images of the devices, the ambient temperature of the device under test must be at least 343 K to obtain high quality images. All temperature rises are referenced to 343 K throughout this work. An Agilent 4155 Semiconductor Parameter Analyzer was used to measure characteristics on the devices.

Gummel characteristics were taken on the measured device in each orientation, while the heat source device was driven at a known power. Infrared images were taken with the measured device off and the heat source at different power levels to determine the temperature gradient across the measured device. Gummel characteristics were then taken

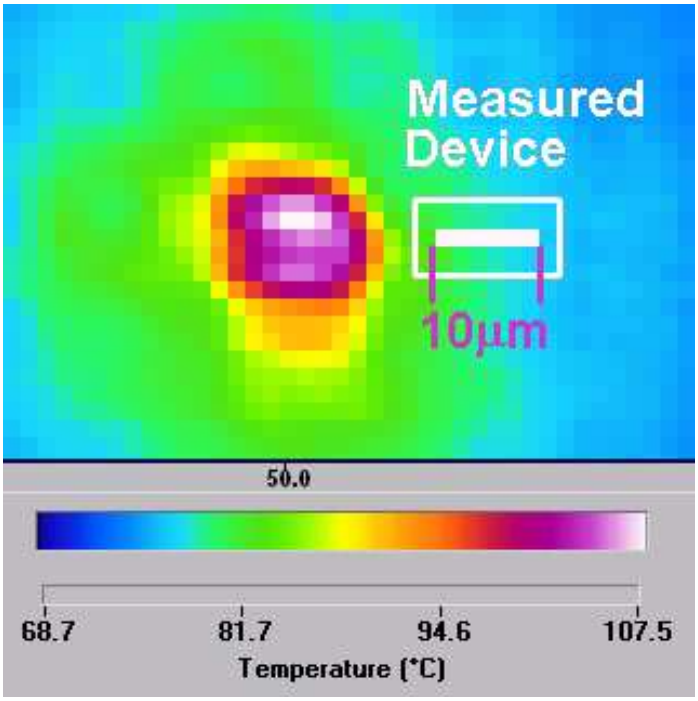

Figure 35: Infrared photo of heat source transistor and thermal distribution that is seen across the measured device.

on the measured device at different ambient temperatures, with the heat source device off, at 4 K increments from 343 K to the maximum temperature measured across the device from the infrared image. Using (12) it was then possible to determine the effective operating temperature of the device at a given I_C, or for the entire Gummel characteristic, as is seen in Figure 36.

5.4 Results

5.4.1 Thermal Correlation

Temperature distribution across the measured devices was found to be significantly different based upon orientation of the devices, as might be expected. The case of the measured devices being horizontal, as in cases b) and c) in Figure 34 is shown in Figure 37. In the $--$ case, the temperature variation across the device, at maximum source power in the adjacent device, is over 12 K and exhibits an exponential type decay. For the $-|$ case, the temperature gradient is not as severe, which is due to the fact that the devices are placed 6 μm further apart. However, the temperature profile across the device exhibits a linear

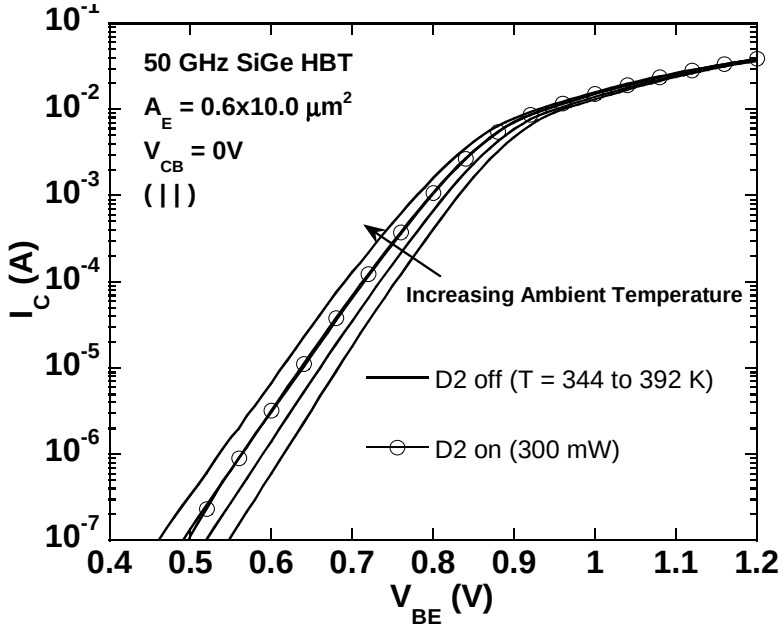

Figure 36: Gummel characteristics on measured device at different ambient temperatures. The characteristic for the measured device operating with the heat source on is superimposed.

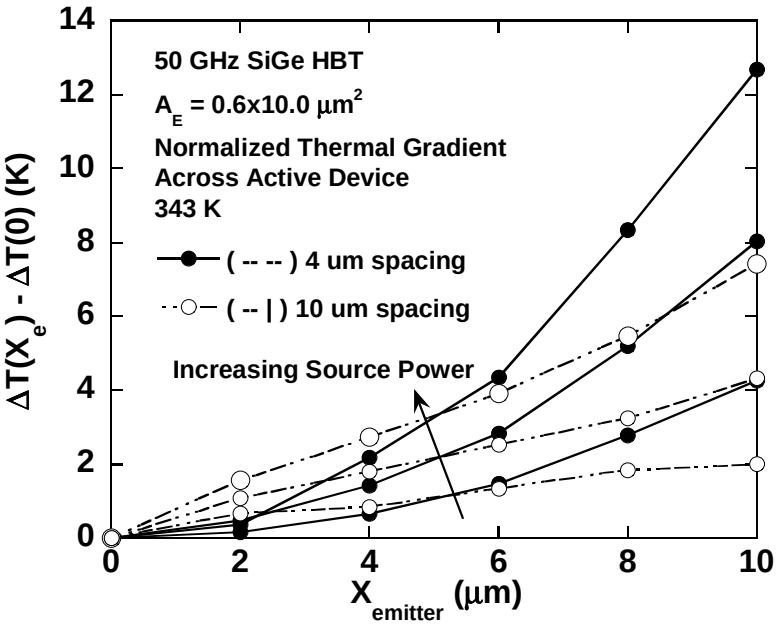

Figure 37: Temperature variations across horizontal measured devices normalized to the minimum temperature rise per configuration.

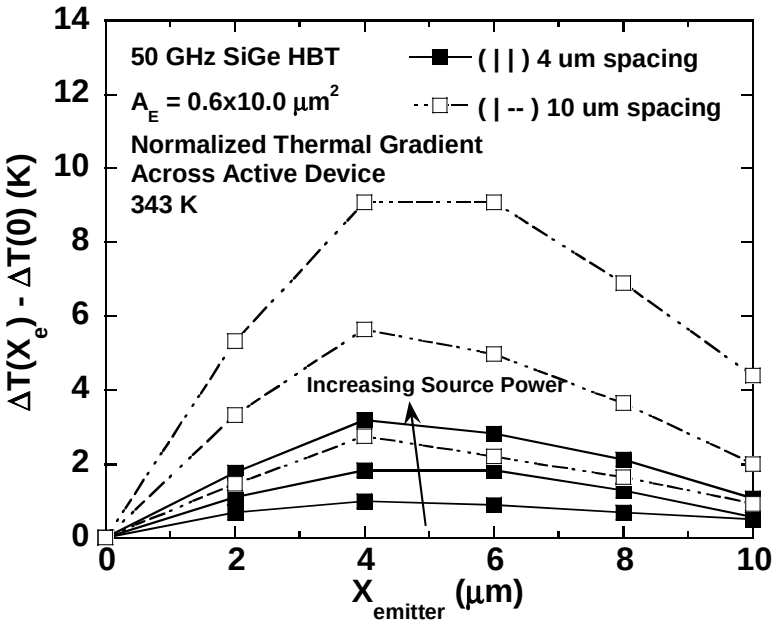

Figure 38: Temperature variations across vertical measured devices normalized to the minimum temperature rise per configuration.

decay. This is due in part to the greater distance from the heat source, and also because the full emitter length is exposed to the measured device within a linear distance on the order of that length. Thus, the unmeasured device can not be treated merely as a point source, as it could have been in the prior case. If the measured device in this orientation were moved closer to the heat source, it would lose some of its linear nature for that of an exponential, but not as much as the $--$ case.

The temperature variation results across the vertically oriented transistors, cases a) and d) in Figure 34, are shown in Figure 38. Both cases exhibit central heating within the device, similar to what one would see due to self heating. The 4 μm spaced $||$ case exhibits the most deviation across the device, mostly due to proximity. The 10 μm $|-$ case does not give much useful information because of its distance from the heat source.

The compilation of measured device temperature rise from ambient temperature as a function of orientation and heat source power from infrared data is shown in Figure 39. The results show that the highest temperature rise is attributed to the $||$ case, which is expected since the greatest device area is visible to the heat source. The $--$ shows the next most temperature rise, which is mainly due to proximity. The other two cases are

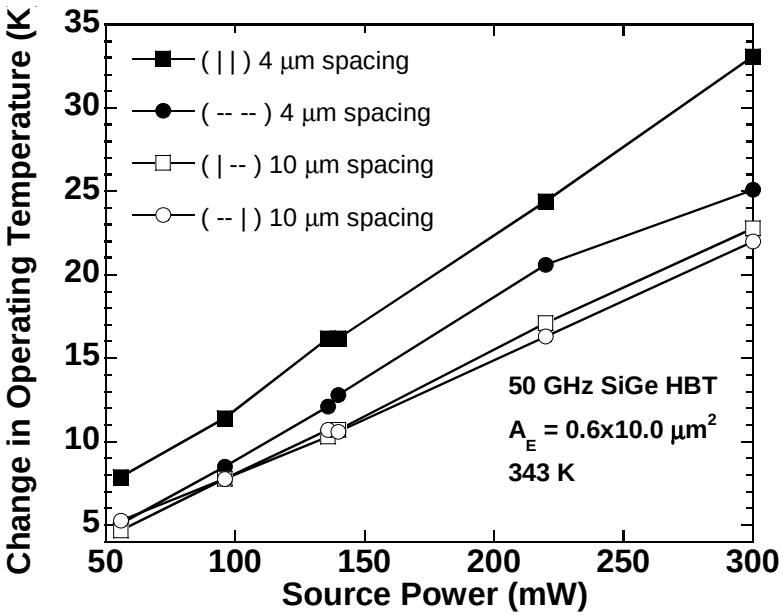

Figure 39: Average infrared measured temperature change vs. heat source power.

hardly distinguishable, mainly due to the fact that the temperature at the 10 μm distance has been well dissipated due to the silicon substrate. The data of Figure 39 is reformatted in Figure 40 to demonstrate that the coupling between the two devices is virtually constant across heat source power, demonstrating a uniform R_{21} per configuration.

Finally, infrared temperature averages are compared to electrically extracted temperatures using (12). The trend of the average infrared temperature and the extracted temperature are consistent across orientation and power. This trend demonstrates that even though wide temperature variations can be seen across the measured device, as was shown in Figures 37 and 38, that the effective device temperature as related to its DC Gummel characteristic is in essence the average temperature across the device. This finding allows for lumped R_{21} electro-thermal modeling for device networks in SiGe without loss of generality.

5.4.2 Breakdown Voltage

The decrease in breakdown voltage with technology scaling in SiGe HBTs (see Figure 33) imposes important constraints on device biasing and operation [59]. Additional measurements were taken to detect any influence on device robustness and breakdown voltage

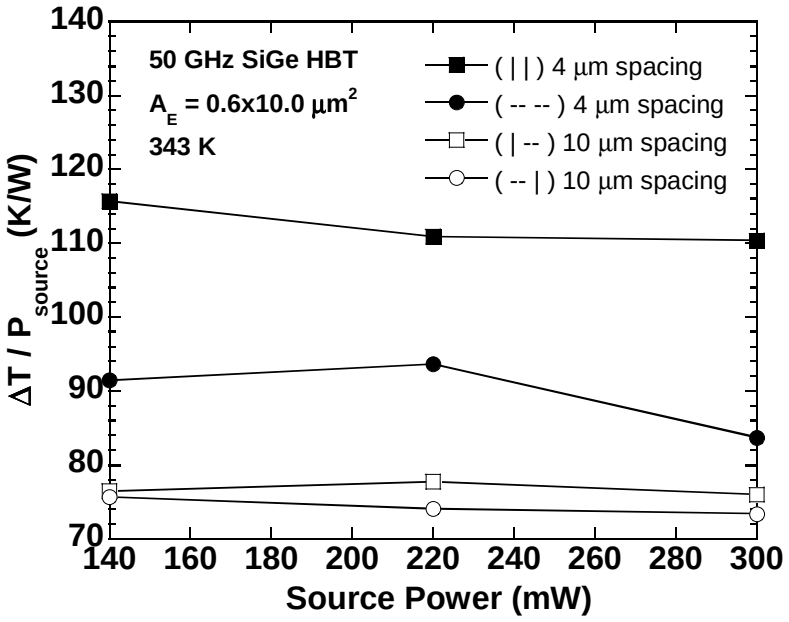

Figure 40: Infrared temperature measured variation independence across heat source power.

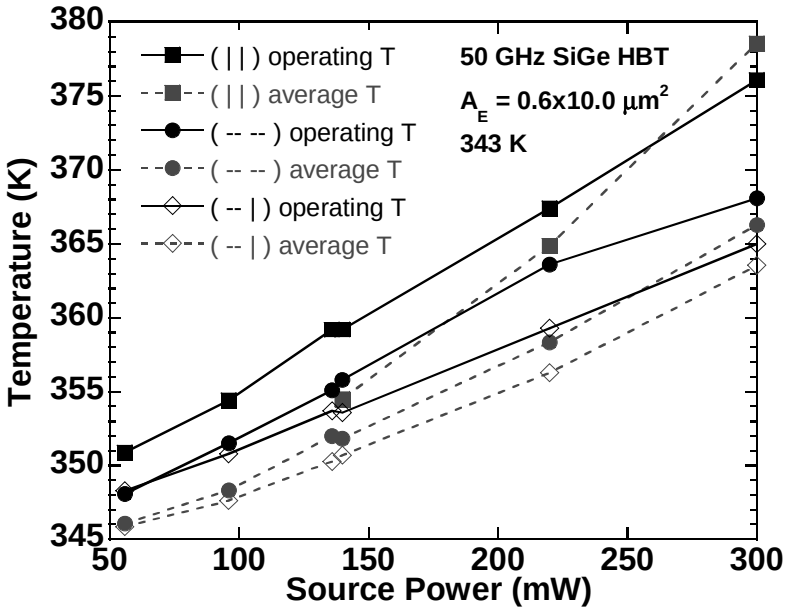

Figure 41: Average infrared measured temperature and electrically extracted temperature of measured device.

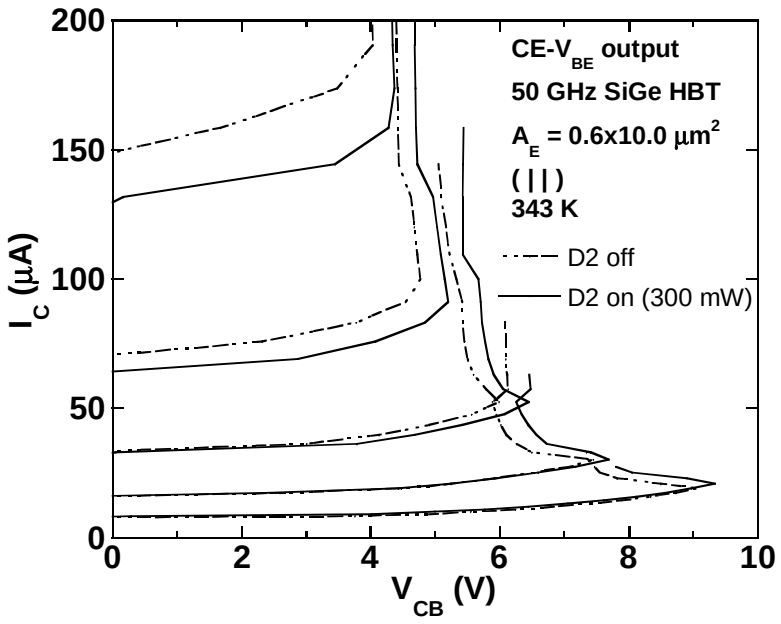

Figure 42: Common emitter output characteristic with forced V_{BE}.

threshold due to emitter thermal gradients from the various layout configurations. Figure 42 shows a common emitter (CE) output characteristic with forced V_{BE}. I_C is swept and V_{CB} monitored to detect the fly-back point, where the device enters electro-thermal runaway. No degradation in the maximum V_{CB} was observed when the heat-source was powered on. In fact, the maximum V_{CB} was observed to be slightly higher in this case, due to the weak decrease in $M - 1$ with increasing temperature. Similarly, safe-operating-area (SOA) characteristics across bias presented in Figure 43 show a slight increase in SOA with the thermal source, and little difference from the case of increased ambient temperature. Results were similar for all layout cases examined. This is clearly good news in terms of device robustness for SiGe HBTs subjected to strong thermal coupling.

5.5 Conclusions

Thermal coupling effects have been studied extensively in technologies with poor thermal conductivity to determine electro-thermal stability of circuits. Not as much work has been done in silicon until recently with the advent of higher power density SiGe technologies. Unlike III-V and SOI technologies, the good thermal conductivity of silicon can keep temperature variations limited to the immediate vicinity of the heat generating source. This,

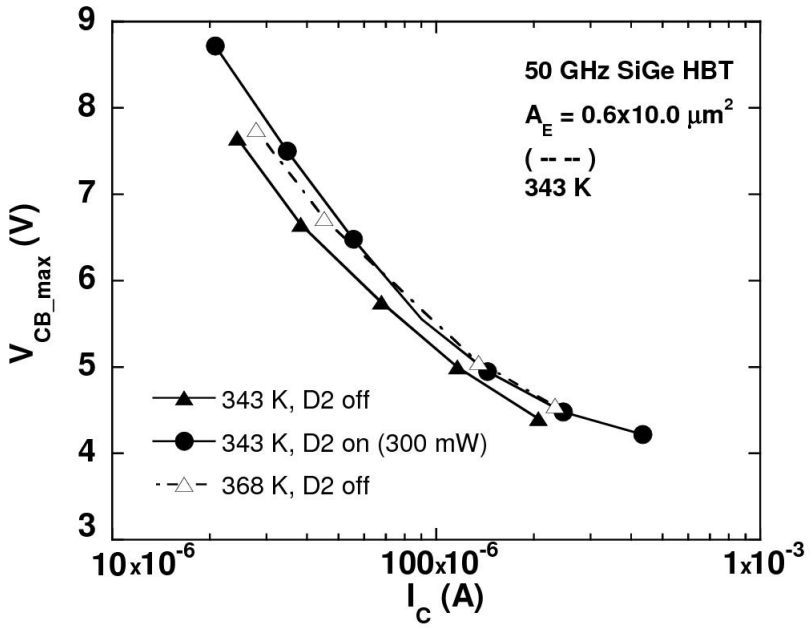

Figure 43: Safe-operating-region characteristics.

however, can present large thermal gradients across devices in close proximity. Through infrared imagery and electrical thermometry, it has been demonstrated that these wide variations need not be treated in a distributed manner, and can still be approximated by a lumped R_{21}. Further, it has been shown that these gradients do not adversely affect such DC characteristics as breakdown voltage. This allows for SiGe designs of multiple transistors to be characterized electro-thermally with multi-port networks, independent of device orientation, without adverse effects to electrical device characteristics.

CHAPTER VI

OPTIMAL THERMAL COUPLING DESIGN

6.1 Introduction

Self-heating within transistors is commonly included in standard bipolar compact models such as VBIC, HiCUM, and MEXTRAM. Failing to properly account for self-heating in high-power circuits such as power amplifiers can compromise the predictive capabilities of such modeling tools. Thermal interactions between high-frequency devices on both SOI [60] and GaAs [61] are well-known to strongly couple to circuit performance due to the poor thermal conduction properties of the respective substrates. While silicon-germanium (SiGe) technology utilizes a silicon substrate that is a much better thermal conductor than either SOI or GaAs, inter-device thermal coupling effects can still be significant [62]. Modeling approaches using both physical models [63] and CAD-assisted techniques [64] have been employed for predicting thermal device interactions, however, most do not lend themselves to popular bipolar models. In general, these techniques have limited value in practical circuit design because they employ either custom models which are tailored for thermal performance, or use simulators which can not easily be incorporated into commercially-available CAD platforms.

Presented here is a technique by which the commonly-used self-heating network in physical bipolar models can be augmented to support mutual thermal coupling, and then applied to optimized power amplifier design. With the addition of an external thermal coupling network, accurate mutual thermal coupling interaction can be predicted using commonly-used IC CAD tools such as *Cadence* and *Spectre*. Using this technique, a multi-transistor SiGe power amplifier cell in a 180 nm, second-generation, 120 GHz peak f_T, SiGe technology is successfully optimized for thermal balance.

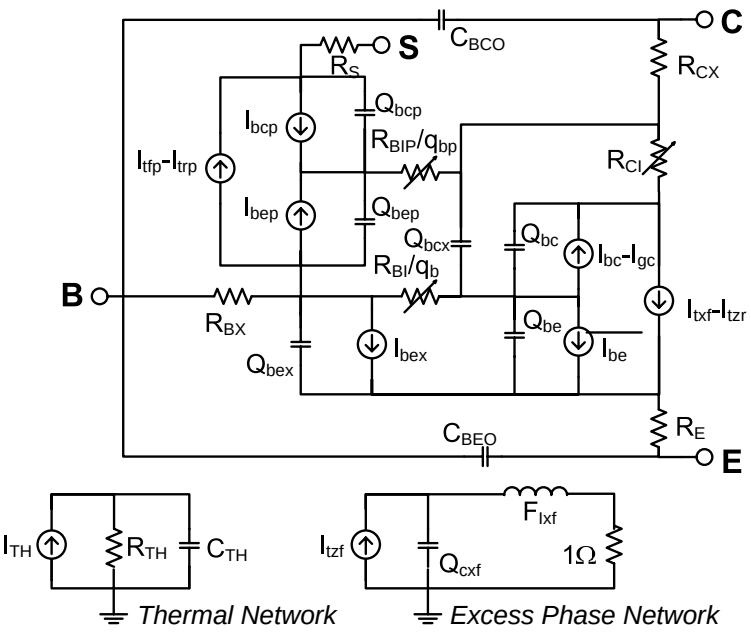

Figure 44: Thermal network commonly employed by compact bipolar models, including VBIC, HiCUM, and MEXTRAM.

6.2 Thermal Networks in Bipolar Models

To account for self-heating effects, many bipolar models employ a thermal network consisting of a parallel combination of thermal resistance, thermal capacitance, and a thermal current source (which represents dissipated power within the transistor). As shown in Figure 44, this thermal network generates a ground-referenced thermal voltage, representing thermal temperature rise within the transistor. This value is then used by other parameters within the model, and through iteration in the solver, a solution for all transistor parameters is achieved.

A commonly-used technique, illustrated in Figure 45, is to represent mutual thermal coupling as voltage sources summed in series with the thermal node of each transistor [65]. While this is the easiest and most physically representative approach, it requires a model which samples and generates its self-heating, T_{S_n}, and total temperature rise (T_n) values at separate nodes. This methodology does not lend itself to standard bipolar compact models because the thermal node is only available as a single reference voltage.

For a model with a single self-heating node to be used experimentally in a mutual

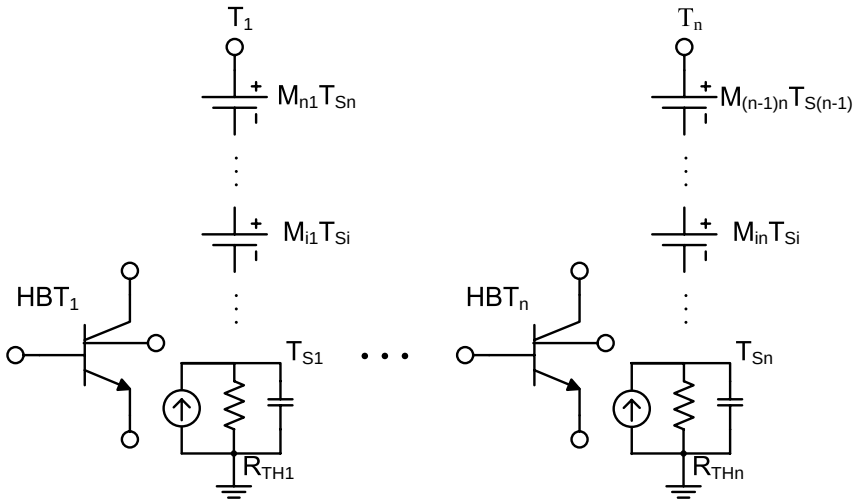

Figure 45: Modeling thermal coupling as summation of thermal potentials.

thermal coupling network, the self-heating and total device heating must be decoupled. The thermal node of the device is used as the total device temperature node and an external network is generated to represent self-heating. The series-connected thermal voltage sources shown in Figure 45 can be replaced by a parallel network of voltage-controlled current sources, whose current is the corresponding thermal voltage T_{S_n} divided by the thermal resistance, R_{TH_n}. A current meter, inserted in series between the mutual coupling current sources and the thermal node, samples the sum of the mutual thermal currents added to the total device temperature node. This current is subtracted from the parallel, current source transformation of the Thevenin equivalent of the total temperature node and the thermal resistance, R_{TH_n}. The equivalent mutual thermal coupling network is shown in Figure 46.

6.3 Model Calibration and Verification

To verify the mutual thermal coupling model, multiple structures consisting of three devices, connected in parallel in a common-base configuration, and placed at varied inter-device spacings, were fabricated and measured. The collectors of the three devices were connected together, but each of the three emitters was available external to the circuit to observe

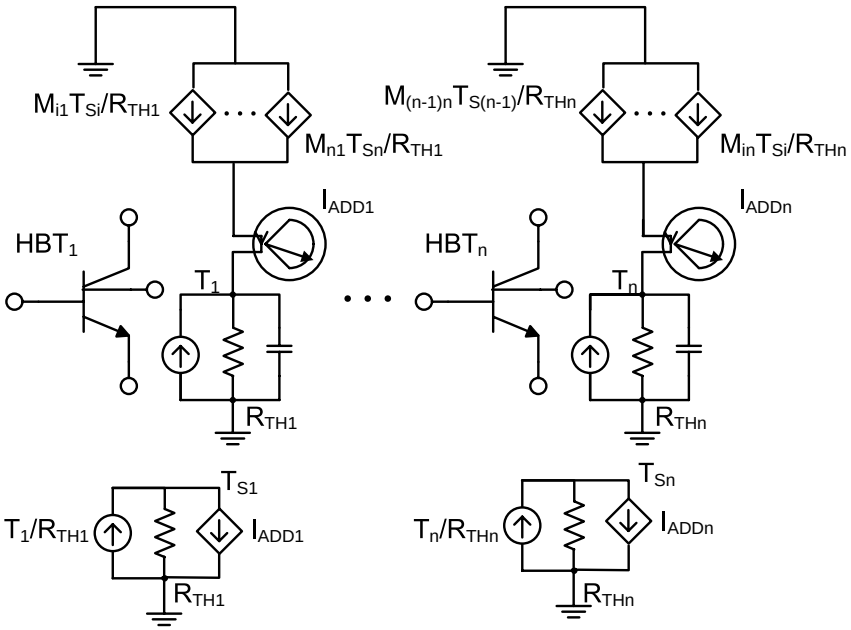

Figure 46: Modeling thermal coupling as summation of thermal currents with separation of self-heating and total device heating nodes.

the current of each device. Current meters were placed in each emitter path to measure the distribution of a common I_E applied to the cell. Various emitter currents, up to three times the peak f_T current for a single device, were applied at varied V_{CB} levels, while the individual device currents were monitored and the temperatures thermally imaged. Utilizing the techniques used in [6], lumped values for mutual coupling M_{ij} were fit to meet both temperature and current distributions.

6.4 Thermal Layout Optimization

Power amplifier cell design is traditionally of great interest in terms of thermal optimization in IC technologies [61][66][67]. Common-base [35] and cascoded amplifiers [2] have demonstrated the ability to increase the standard breakdown voltage over that of a conventional common-emitter configuration. This approach beneficially increases the power output of a device, but negatively impacts the power dissipation and operating temperature, worsening the effects of thermal coupling. Ignoring unequal current distributions resulting from thermal in-balance in SiGe PAs has been shown to decrease power amplifier gain and output

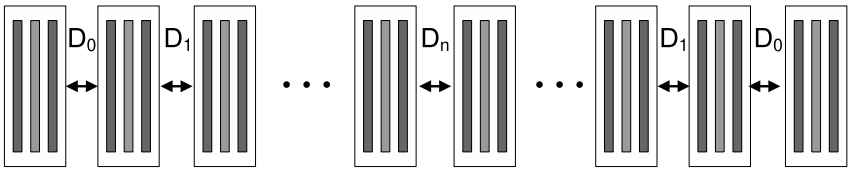

Figure 47: Linear transistor layout for first-order thermal optimization of power cell transistors electrically connected in parallel.

power by a factor of multiple dB and also impact PAE by over 10% [57]. Varying the emitter spacing within a multi-finger device has been shown to effectively thermally balance a single power device [57]. Here, this technique is extrapolated to a multi-device PA cell instead of a multi-finger one.

The power amplifier structure targeted for optimization consists of multiple thermally-coupled transistors connected in parallel in a common-base configuration, spaced in a linear array, as shown in Figure 47. For an array of N devices, it is possible to balance the temperature across the internal $N-2$ devices by varying the inter-device spacing. The outer two devices will always have a lower temperature than the inner devices since they have only one directly adjacent heat source. Consequently, the D_0 spacing shown in Figure 47 is set to the minimum device spacing rule set forth in the design kit.

The remaining spacings were optimized using Newton's method. For single dimensional arrays, the standard set of equations used for determining the iterative Newton step as a function of first and second order derivatives are shown in equations (13) - (15).

$$f(x+h) \simeq f(x) + f'(x)h + \frac{f''(x)}{2}h^2 \tag{13}$$

$$h = -\frac{f'(x)}{f''(x)} \tag{14}$$

$$x_{k+1} = x_k - \frac{f'(x)}{f''(x)} \tag{15}$$

Lacking empirical models for differentiation, numerical differentiation through small Δ's around the absolute spacing of each transistor were calculated. For two dimensional optimization (such as cascode amplifiers), the Jacobian must be employed through the use of equations (16) - (17).

$$\bar{\mathbf{x}}_{k+1} = \bar{\mathbf{x}}_k - \nabla f(\bar{\mathbf{x}}_k) H^{-1}(\bar{\mathbf{x}}_k) \tag{16}$$

$$H(\bar{\mathbf{x}}) = \left[\frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_i \partial x_j}\right] = \begin{bmatrix} \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_1 \partial x_1} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_1 \partial x_j} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_1 \partial x_N} \\ \vdots & & \vdots & & \vdots \\ \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_i \partial x_1} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_i \partial x_j} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_i \partial x_N} \\ \vdots & & \vdots & & \vdots \\ \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_N \partial x_1} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_N \partial x_j} & \cdots & \frac{\partial^2 f(\bar{\mathbf{x}})}{\partial x_N \partial x_N} \end{bmatrix} \tag{17}$$

Bounding and reduced scaling of iterate Newton steps were employed to improve solution stability while sacrificing convergence speed. Minimum device spacing for all D_n was used as an initial seed. For the inner $N-2$ devices, each possessing a given temperature T_n, a suitable cost function for temperature minimization is:

$$T_{cost} = \sum_{i=2}^{N-2} \sum_{j=i+1}^{N-1} (T_j - T_i)^2 \tag{18}$$

Table 4: Device temperatures for minimally and optimally spaced power amplifier cells consisting of 6 and 8 devices, with optimal inter-device spacing (minimal spacing is 4μm).

Device	6 Min °C	6 Opt °C	Gap μm	8 Min °C	8 Opt °C	Gap μm
1	37.3	33.8		36.6	33.6	
2	45.0	39.9	4.00	44.1	39.8	4.00
3	47.8	39.3	4.54	47.8	40.1	4.26
4	48.3	38.9	13.52	49.9	38.8	10.18
5	44.6	40.7	4.54	49.3	39.2	8.86
6	36.5	35.0	4.00	48.2	40.1	10.18
7				44.4	40.3	4.26
8				36.8	34.5	4.00

This cost function ensures that all temperature differences between devices are positive, allowing for Newton's method to solve the matrix through minimization.

6.5 SiGe PA Cell Design

A unit 0.2 x 20 μm emitter area compact device model within a commercially-available 120 GHz SiGe process was modified to have access to its thermal port. Power cells consisting of six and eight unit devices, resulting in two and three inter-device spacings for optimization, respectively, were connected in parallel in a common-base configuration. An external mutual thermal coupling network employing a low-order, polynomial temperature distribution model was then generated. The network was driven with a V_{CE} of 2.0 Volts and an I_E equal to the number of devices times the peak f_T of the unit device. A transistor array with optimal device spacings and a control array with minimum device spacings were fabricated and measured.

6.6 Measured Results

Measured device temperature rises are listed in Table 4 for both the six and eight device power cells, and a plot of the minimum and optimum eight device cells is shown in Figure 48.

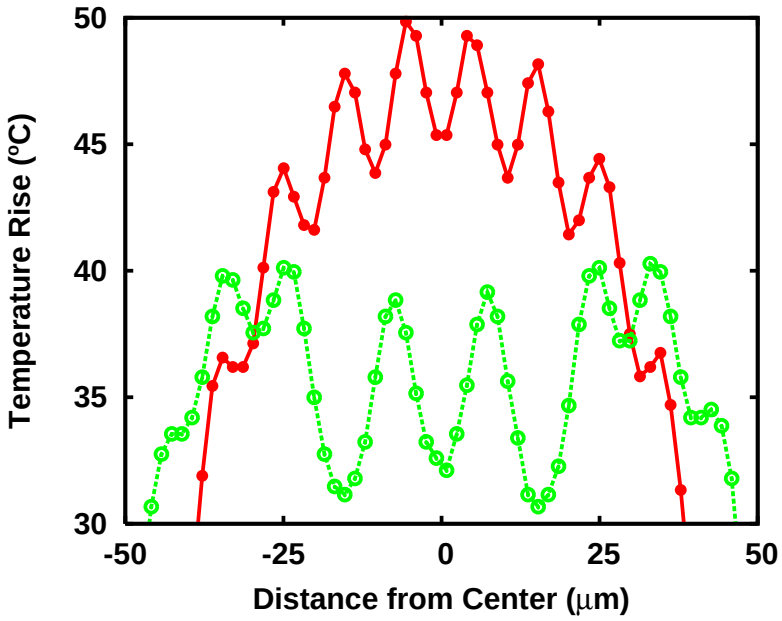

Figure 48: An 8-transistor coupling temperature rise for minimally (closed circle) and optimally designed (open circle) spaced power cell, driven at an emitter current of 250 mA (8 times the peak f_T current for an individual device) and a V_{CB} of 2.2 Volts.

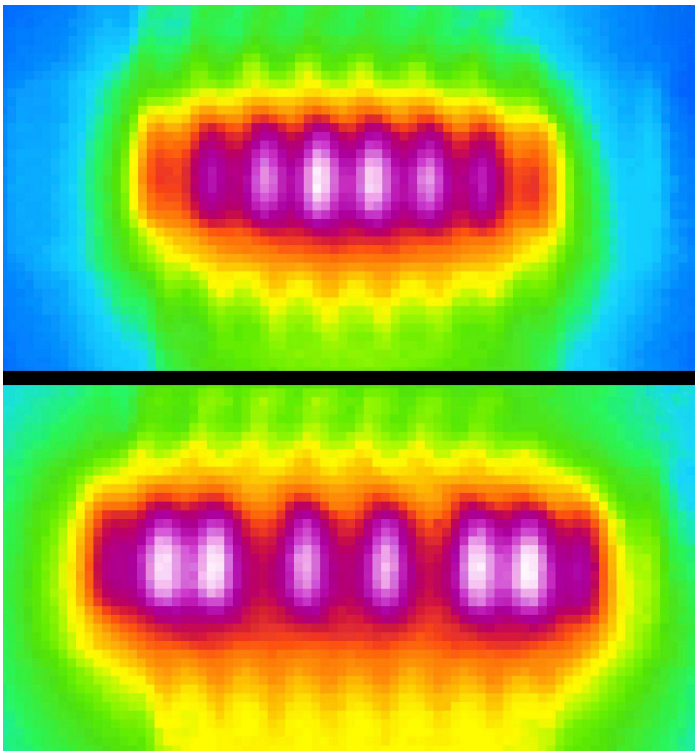

Figure 49: 8 device coupling thermal photo for both minimum (top) and optimized spacings (bottom).

An infrared photo of the eight device configurations for minimal and optimal spacings is shown in Figure 49. The optimum spacing configuration for the eight device cell yielded an average temperature rise across the six inner devices of 39.9 °C, with a standard deviation of 0.4 °C. This average temperature rise represents a 10.0 °C decrease in temperature relative to the peak temperature rise seen in the minimum spacing configuration.

6.7 Summary

While mutual thermal coupling models have been previously developed for use in specialized simulators, it remains difficult to implement in standard CAD platforms using compact models provided in standard IC design kits. Utilizing a thermal coupling network that is compliant with single port self-heating models and an appropriate thermal coupling distribution network, a simple technique for implementing mutual thermal coupling has been demonstrated. Implementing standard optimization techniques has resulted in successful

temperature balancing of both six and eight device transistor arrays in a 120 GHz SiGe technology. This procedure offers a straightforward technique for circuit designers to simulate mutual thermal coupling within their circuit designs with simple modifications to existing transistor models provided by the IC foundry.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

The contributions of this work are:

1. First introduction of the mixed breakdown cascode architecture for SiGe to increase both breakdown voltage and gain simultaneously. (Chapter II).

2. Implementation of the mixed breakdown cascode architecture in a two-stage amplifier with greater than 40 dB of gain. To the best of the author's knowledge, this is the highest gain per stage amplifier at X-Band in existence today across all published technologies (Chapter III).

3. Implementation of the mixed breakdown cascode architecture in a near one Watt output power amplifier. To the best of the author's knowledge, this represents the highest output power in SiGe achieved at the time of publishing (Chapter IV).

4. Demonstration that as a function of spacing rules in commercially available SiGe design kits that a lumped mutual thermal impedance is valid, irrespective of device orientation (Chapter V).

5. Implementation of a supplementary model producing program which is easily integrated with commercially available design software to effectively model mutual thermal coupling between devices in a multi-transistor array in SiGe. Furthermore, device optimization through the use of Newton's method was used to effectively thermally balance an array of transistors in a SiGe process (Chapter VI).

In the future, this work can be extended by:

1. Completing the full output match of the high power amplifier across the 8.5 to 10.5 GHz portion of the X-Band.

2. Improving the high output power amplifier through the use of higher power core devices to improve efficiency and minimize parasitics.

3. Augmenting the thermal balance findings through AC and load pull measurements on PA cells.

4. Improving the efficiency and stability of the high output power amplifier through thermal optimization.

5. Implementing the mixed cascode architecture at mm-wave frequencies and above.

6. Improving the convergence algorithms of the thermal optimization routines.

APPENDIX A

PROGRAM LISTING - NETLIST_BUILDER.C

`netlist_builder.c` takes a netlist file formatted for *Spectre* analysis and inserts the augmented thermal network shown in Figure 46. Following is a description of what the individual functions within the program do.

`get_ln(...)` parses the input file into readable lines used by other functions.

`get_strings(...)` parses a single line from the inputted file into keywords, variables, and numerical values which are used to analyze the device and nodes for insertion of additional components.

`model_inc(...)` automatically increments the inserted models to unique identifier values.

`main(..)` inputs the netlist file and passes it to the above procedures to parse it into readable models for future use. It does some housekeeping formatting, presenting the appropriate directories for the models to use. It then renames every transistor to a unique identifier. Following this, it then inserts a zero voltage source to sense the input current, generates an external network to renormalize the internally generated temperature, and inserts a thermal resistor and a variable transconductance which will be altered by `iterator_gen.c`.

Program Listing:

```
#include <stdio.h>
#include <ctype.h>
#include <string.h>
```

```
int get_ln(char *line,FILE *file)
{
     char temp_read;
     int char_count=0;

     temp_read=fgetc(file);
     while(temp_read!='\n'&&temp_read!=EOF)
     {
          line[char_count]=temp_read;
          char_count++;
          temp_read=fgetc(file);
     }
     line[char_count]='\0';

     if(temp_read==EOF)
          return(0);
     else
          return(1);
}

int get_strings(char *my_read_line,char my_strings[][100])
{
     int string_count=0,char_count=0,in_string_count=0;

          while(char_count<strlen(my_read_line))
          {
               if(isalpha(my_read_line[char_count]))
               {
```

```
        my_strings[string_count][in_string_count]=
        my_read_line[char_count];
        char_count++;
        in_string_count++;
        while(isalnum(my_read_line[char_count])
        ||my_read_line[char_count]=='_')
        {
            my_strings[string_count][in_string_count]=
            my_read_line[char_count];
            char_count++;
            in_string_count++;
        }
        my_strings[string_count][in_string_count]='\0';
        string_count++;
        in_string_count=0;
    }
    else if(isdigit(my_read_line[char_count]))
    {
        my_strings[string_count][in_string_count]=
        my_read_line[char_count];
        char_count++;
        in_string_count++;
        while(isdigit(my_read_line[char_count]))
        {
            my_strings[string_count][in_string_count]=
            my_read_line[char_count];
            char_count++;
            in_string_count++;
        }
```

```
        my_strings[string_count][in_string_count]='\0';
        string_count++;
        in_string_count=0;
    }
    else if(isspace(my_read_line[char_count]))
    {
        my_strings[string_count][in_string_count]=
        my_read_line[char_count];
        char_count++;
        in_string_count++;
        while(isspace(my_read_line[char_count]))
        {
            my_strings[string_count][in_string_count]=
            my_read_line[char_count];
            char_count++;
            in_string_count++;
        }
        my_strings[string_count][in_string_count]='\0';
        string_count++;
        in_string_count=0;
    }
    else if(ispunct(my_read_line[char_count]))
    {
        my_strings[string_count][in_string_count]=
        my_read_line[char_count];
        char_count++;
        in_string_count++;
        while(ispunct(my_read_line[char_count]))
        {
```

```
                    my_strings[string_count][in_string_count]=
                    my_read_line[char_count];
                    char_count++;
                    in_string_count++;
               }
               my_strings[string_count][in_string_count]='\0';
               string_count++;
               in_string_count=0;
          }
          else
          {
          }
     }
     return(string_count);
}

void model_inc(char *model_item)
{
     model_item[0]++;
     if(model_item[0]=='z')
     {
          model_item[0]='a';
          model_item[1]++;
     }
}

#define NETSTART 100
#define RTH 1116.48
#define NETPADJ 200
```

```
#define NETAMM 300


int main(int argc, char *argv[ ])
{
     FILE *infile,*outfile;
     char infilename[100],outfilename[100];
     char infileline[255],infilestrings[100][100];
     int num_strings,loop,loop1,loop_remain,q_count=0,q_flag,g_count;

     if(argc<3)
       {
       printf("usage: %s infilename outfilename\n",argv[0]);
       exit(0);
       }
     else
       {
         strcpy(infilename,argv[1]);
         strcpy(outfilename,argv[2]);
       }

     infile=fopen(infilename,"r");
     outfile=fopen(outfilename,"w");

           while(get_ln(infileline,infile))
       {
         loop_remain=0;
         num_strings=get_strings(infileline,infilestrings);

         if(num_strings>0&&strcmp(infilestrings[0],"global")==0)
```

```
  {
 for(loop=0;loop<num_strings;loop++)
   fprintf(outfile,"%s",infilestrings[loop]);

 fprintf(outfile,"\n");
 loop_remain=num_strings;
 fprintf(outfile,"CircInfo info what=models where=file file=
 \"%%C:r.info\" extremes=no detail=node\n");
  }

if(num_strings>0&&strcmp(infilestrings[0],"include")==0)
  {
 fprintf(outfile,"include \"~/7hp/thermal_models/
 allModels.scs\"\n");
 fprintf(outfile,"//");
  }

q_flag=1;
if(num_strings>0&&infilestrings[0][0]=='Q')
  {
 loop=1;
 while(loop<strlen(infilestrings[0])&&q_flag==1)
   {
     if(!isdigit(infilestrings[0][loop]))
     {
        q_flag=0;
     }
     loop++;
   }
```

```
  }

if(num_strings>0&&infilestrings[0][0]=='Q'&&q_flag==1)
  {
 while(infilestrings[loop_remain][0]!=')')
   {
     fprintf(outfile,"%s",infilestrings[loop_remain]);
     loop_remain++;
   }
 fprintf(outfile," net%i",NETSTART+q_count);
 q_count++;
  }

if(num_strings>0&&strncmp(infilestrings[0],"simulator",9)==0)
  {
 g_count=0;
 for(loop=0;loop<q_count;loop++)
   {
     fprintf(outfile,"V%i (net%i net%i) vsource dc=0.0 type=dc\n",
     NETSTART+loop,NETAMM+loop,NETSTART+loop);
     fprintf(outfile,"G%i (0 net%i net%i 0) vccs gm=%lg\n",g_count,
     NETPADJ+loop,NETSTART+loop,1.0/RTH);
     fprintf(outfile,"F%i (net%i 0) cccs gain=1.0 probe=V%i\n",loop,
     NETPADJ+loop,NETSTART+loop);
     fprintf(outfile,"R%i (net%i 0) resistor r=%lg\n",NETSTART+loop,
     NETPADJ+loop,RTH);
     g_count++;
     for(loop1=0;loop1<q_count;loop1++)
       {
```

```
                if(loop!=loop1)
                  {
                    fprintf(outfile,"G%i (0 net%i net%i 0) vccs gm=0.00001\n",
                    g_count,NETAMM+loop,NETPADJ+loop1);
                    g_count++;
                  }
                 }
             }
            }

          for(loop=loop_remain;loop<num_strings;loop++)
            fprintf(outfile,"%s",infilestrings[loop]);
          fprintf(outfile,"\n");
        }

      fclose(infile);
      fclose(outfile);
}
```

APPENDIX B

PROGRAM LISTING - ITERATOR_GEN.C

`iterator_gen.c` takes as its input the thermally augmented file which is generated by `netlist_builder.c`, a file with initial temperature seeds, and a target threshold for the temperature error amongst the inner devices of the array. It makes iterative system calls to *Spectre* to evaluate the cost function to determine the temperature errors amongst the inner devices as well as determining temperature deltas to calculate discrete derivatives used in Newton's minimization method to converge on a solution. Following is a description of what the individual functions within the program do.

`get_ln(...)` parses the input file into readable lines used by other functions.

`get_strings(...)` parses a single line from the inputted file into keywords, variables, and numerical values which are used to analyze the device and nodes for insertion of additional components.

`read_q_file(...)` reads in the initial temperature and spacing seed values for transistor spacings.

`new_update_pos(...)` updates the positions of the devices in the transistor array as a function of the most current Newton step.

`new_dev_distance(...)` calculates the distance between any two devices in the optimization array.

`new_calc_cost(...)` determines the temperature difference between all devices being optimized in the array and squares the value to make it minimizable by Newton's method.

`update_list(...)` updates the transistor array list per iteration.

`calc_casc_cost(...)` calculates the cost function in the case of a cascoded structure.

`inverse(...)` inverts a square matrix passed to it.

`get_q(...)` reads the transistor data file.

`gm_file_change(...)` updates the g_m values to be used in the augmented model file based upon the Newton calculations. This file will then be used by *Spectre* to calculate the next set of system parameters.

`get_temps(...)` reads the temperatures from the seed file.

`get_cost(...)` calls *Spectre* externally, using the iterated placements and calculates the new cost temperature.

`array_col_nult(...)`, `row_array_mult(...)`, `col_row_mult(...)`, `row_col_mult(...)`, `array_array_mult(...)`, `array_scalar_mult(...)`, and `array_array_add(...)` all perform mathematical functions on arrays that are described by their names. These are generally used in the Newton step calculations.

`newton_derivatives(..)` determines discrete derivatives used by Newton's method to minimize the temperatures in the array.

`get_seeds(...)` reads the seed file.

`main(...)` calls the above listed functions to read in the augmented thermal model file, the seed file and the desired threshold. It then iterates on the configuration, updating the spacings with Newton steps as calculated by discrete derivatives through system calls to *Spectre*. When the temperature threshold is reached, the spacings are outputed.

Program Listing:

```
#include <stdio.h>
#include <ctype.h>
#include <string.h>
#include <math.h>
#include <stdlib.h>

struct transistor{
  char name[10];
  double x;
  double y;
};

struct gaps{
  char type;
  char dev[2][10];
};

int get_ln(char *line,FILE *file)
{
     char temp_read;
     int char_count=0;
```

```
     temp_read=fgetc(file);
     while(temp_read!='\n'&&temp_read!=EOF)
     {
          line[char_count]=temp_read;
          char_count++;
          temp_read=fgetc(file);
     }
     line[char_count]='\0';

     if(temp_read==EOF)
          return(0);
     else
          return(1);
}

int get_strings(char *my_read_line,char my_strings[][100])
{
     int string_count=0,char_count=0,in_string_count=0;

          while(char_count<strlen(my_read_line))
          {
               if(isalpha(my_read_line[char_count]))
               {
                    my_strings[string_count][in_string_count]=
                    my_read_line[char_count];
                    char_count++;
                    in_string_count++;
                    while(isalnum(my_read_line[char_count])
```

```
     ||my_read_line[char_count]=='_')
     {
          my_strings[string_count][in_string_count]=
          my_read_line[char_count];
          char_count++;
          in_string_count++;
     }
     my_strings[string_count][in_string_count]='\0';
     string_count++;
     in_string_count=0;
}
else if(isdigit(my_read_line[char_count]))
{
     my_strings[string_count][in_string_count]=
     my_read_line[char_count];
     char_count++;
     in_string_count++;
     while(isdigit(my_read_line[char_count]))
     {
          my_strings[string_count][in_string_count]=
          my_read_line[char_count];
          char_count++;
          in_string_count++;
     }
     my_strings[string_count][in_string_count]='\0';
     string_count++;
     in_string_count=0;
}
else if(isspace(my_read_line[char_count]))
```

```
{
     my_strings[string_count][in_string_count]=
     my_read_line[char_count];
     char_count++;
     in_string_count++;
     while(isspace(my_read_line[char_count]))
     {
          my_strings[string_count][in_string_count]=
          my_read_line[char_count];
          char_count++;
          in_string_count++;
     }
     my_strings[string_count][in_string_count]='\0';
     string_count++;
     in_string_count=0;
}
else if(ispunct(my_read_line[char_count]))
{
     my_strings[string_count][in_string_count]=
     my_read_line[char_count];
     char_count++;
     in_string_count++;
     while(ispunct(my_read_line[char_count]))
     {
          my_strings[string_count][in_string_count]=
          my_read_line[char_count];
          char_count++;
          in_string_count++;
     }
```

```
                    my_strings[string_count][in_string_count]='\0';
                    string_count++;
                    in_string_count=0;
               }
               else
               {
               }
          }
          return(string_count);
}

void read_q_file(FILE *infile,struct transistor *devices,
struct transistor *cost_devices,struct gaps *all_gaps,int *num_devices,
int *num_gaps,int *num_cost_devices)
{
  char read_line[255],temp_char,read_strings[50][100];
  int num_strings,counter,devs;

  *num_gaps=0;
  *num_devices=0;
  *num_cost_devices=0;

  while(get_ln(read_line,infile))
    {
      num_strings=get_strings(read_line,read_strings);

      if(read_line[0]=='Q')
     {
       sscanf(read_line,"%s %lg %lg",&devices[*num_devices].name,
```

```
  &devices[*num_devices].x,&devices[*num_devices].y);
  *num_devices+=1;
}

 if(strncasecmp(read_line,"gap",3)==0)
{
  all_gaps[*num_gaps].type=read_line[3];
  counter=1;
  devs=0;
  all_gaps[*num_gaps].dev[0][0]='\0';
  all_gaps[*num_gaps].dev[1][0]='\0';

  while(counter<num_strings)
    {
      if(!isspace(read_strings[counter][0]))
     {
       strcpy(all_gaps[*num_gaps].dev[devs],read_strings[counter]);
       devs++;
     }
      counter++;
    }

  *num_gaps+=1;
}

 if(strncasecmp(read_line,"cost",4)==0)
{
  counter=1;
  while(counter<num_strings)
```

```
          {
            if(!isspace(read_strings[counter][0]))
           {
             strcpy(cost_devices[*num_cost_devices].name,
             read_strings[counter]);
             *num_cost_devices+=1;
           }
            counter++;
          }
     }


    }
}

void new_update_pos (struct transistor *devices,struct gaps *all_gaps,
int num_devices,int which_gap,double delta)
{
  int loop,loop1;
  double x_val;
  switch(all_gaps[which_gap].type)
    {
    case 'X':
      for(loop=0;loop<2;loop++)
     {
       loop1=0;
       while(strcasecmp(devices[loop1].name,all_gaps[which_gap].dev[loop])
       !=0&&loop1<num_devices)
         loop1++;
       if(loop1<num_devices)
```

```
          {
            x_val=devices[loop1].x;
            for(loop1=0;loop1<num_devices;loop1++)
           if(devices[loop1].x>=x_val)
             devices[loop1].x+=delta;
          }
      }
       break;

     case 'Y':
       for(loop=0;loop<2;loop++)
      {
        loop1=0;
        while(strcasecmp(devices[loop1].name,all_gaps[which_gap].dev[loop])
        !=0&&loop1<num_devices)
          loop1++;
        if(loop1<num_devices)
          {
            devices[loop1].y+=delta;
          }
      }
       break;

     default:
       break;
     }
}

double new_dev_distance(struct transistor *device,int dev1,int dev2)
```

```
{
  int loop=0,loop1=0;

  while(atoi(device[loop].name+1)!=dev1)
    loop++;

  while(atoi(device[loop1].name+1)!=dev2)
    loop1++;

  return(sqrt(pow(device[loop].x-device[loop1].x,2)+pow(device[loop].y-
  device[loop1].y,2)));
}

double new_calc_cost(double *temps, struct transistor *cost_devices,
int num_cost_devices)
{
  double cost_val=0.0;
  int loop,loop1,dev1,dev2;

  for(loop=0;loop<num_cost_devices-1;loop++)
    for(loop1=loop+1;loop1<num_cost_devices;loop1++)
      {
     dev1=atoi(cost_devices[loop].name+1);
     dev2=atoi(cost_devices[loop1].name+1);
     cost_val+=pow(temps[dev1]-temps[dev2],2);
      }

  return(cost_val);
}
```

```
void update_list(double *dist_list,int list_size,int gap, double value)

{
  dist_list[gap]=value;
  dist_list[list_size-gap-1]=value;
}

double calc_casc_cost(double *temps,int size)
{
  double cost_val=0.0;
  int loop,loop1;

  for(loop=0;loop<2*(size-1);loop+=2)
    for(loop1=loop+2;loop1<2*size;loop1+=2)
      cost_val+=pow(temps[loop]-temps[loop1],2);
  return(cost_val);
}

#define NETSTART 100
#define MAXARRAY 20
#define NETPADJ 200
#define NETAMM 300

void inverse (double array[][MAXARRAY],int array_size)
{
  double local_array[MAXARRAY][2*MAXARRAY],pivot;
  int loop,loop1,loop2;
```

```
for(loop=0;loop<array_size;loop++)
  for(loop1=0;loop1<array_size;loop1++)
    local_array[loop][loop1]=array[loop][loop1];


for(loop=0;loop<array_size;loop++)
  for(loop1=0;loop1<array_size;loop1++)
    {
   if(loop==loop1)
     local_array[loop][loop1+array_size]=1.0;
   else
     local_array[loop][loop1+array_size]=0.0;
    }


for(loop=0;loop<array_size;loop++)
  {
    pivot=local_array[loop][loop];


    for(loop1=loop;loop1<array_size*2;loop1++)
   local_array[loop][loop1]/=pivot;


    for(loop1=loop+1;loop1<array_size;loop1++)
   {
       pivot=local_array[loop1][loop];


       for(loop2=loop;loop2<2*array_size;loop2++)
         {
        local_array[loop1][loop2]-=local_array[loop][loop2]*pivot;
         }
   }
```

```
    }

  for(loop=array_size-1;loop>0;loop--)
    {
      for(loop1=loop-1;loop1>=0;loop1--)
     {
       pivot=local_array[loop1][loop];

       for(loop2=loop;loop2<2*array_size;loop2++)
         {
           local_array[loop1][loop2]-=local_array[loop][loop2]*pivot;
         }
     }
    }

  for(loop=0;loop<array_size;loop++)
    for(loop1=0;loop1<array_size;loop1++)
      array[loop][loop1]=local_array[loop][loop1+array_size];
}

int get_q(char *infilename)
{
  char infileline[255],infilestrings[100][100];
  int num_strings,loop,num_q=0;
  FILE *infile;

  infile=fopen(infilename,"r");

  while(get_ln(infileline,infile))
```

```
    {
      num_strings=get_strings(infileline,infilestrings);

      if(num_strings>0&&infilestrings[0][0]=='Q')
     {
       num_q++;
     }
    }
  fclose(infile);

  return(num_q-1);
}

#define RTH 1116.48
#define M -0.07156168
#define B -0.532378616

void gm_file_change(char *infilename,struct transistor *device)
{
  char outfilename[100];
  char infileline[255],infilestrings[100][100],sys_com[100];
  int num_strings,loop_remain,dev_count,dev1,dev2,loop;
  FILE *infile,*outfile;
  double gm=1/RTH;

  sprintf(outfilename,"temp.out");

  infile=fopen(infilename,"r");
  outfile=fopen(outfilename,"w");
```

```
while(get_ln(infileline,infile))
  {
    loop_remain=0;
    num_strings=get_strings(infileline,infilestrings);
    dev_count=0;

    if(num_strings>0&&infilestrings[0][0]=='G')
   {
     while(strcmp(infilestrings[loop_remain],"gm")!=0)
       {
         if(strncmp(infilestrings[loop_remain],"net",3)==0)
        {
          if(dev_count==0)
            dev1=atoi(infilestrings[loop_remain]+3);
          else
            dev2=atoi(infilestrings[loop_remain]+3);
          dev_count++;
        }

         fprintf(outfile,"%s",infilestrings[loop_remain]);
         loop_remain++;
       }
     if(dev1>=NETAMM)
       {
            fprintf(outfile,"gm=%lg",gm*exp(B)*exp(M*new_dev_distance(
            device,dev1-NETAMM,dev2-NETPADJ)));

       loop_remain=num_strings;
```

```
          }
      }

       for(loop=loop_remain;loop<num_strings;loop++)
      fprintf(outfile,"%s",infilestrings[loop]);
       fprintf(outfile,"\n");
     }

      fclose(infile);
      fclose(outfile);

      sprintf(sys_com,"cp temp.out %s",infilename);
      system(sys_com);
      sprintf(sys_com,"rm temp.out");
      system(sys_com);
}

void get_temps(double *temps,int size)
{
  char infileline[255],infilestrings[100][100];
  int num_strings;
  FILE *infile;

  infile=fopen("spectre.dc","r");

  while(get_ln(infileline,infile))
    {
      num_strings=get_strings(infileline,infilestrings);
```

```
      if(num_strings>0&&strncmp(infilestrings[0],"net",3)==0)
     {
       if(atoi(infilestrings[0]+3)>=NETSTART&&atoi(infilestrings[0]+3)<
       NETSTART+size)
         temps[atoi(infilestrings[0]+3)-NETSTART]=atof(infileline+6);
     }
    }

  fclose(infile);
}

double get_cost(char *infilename,struct transistor *device,int size,
 struct transistor *cost_devices,int num_cost_devices)
{
  char sys_com[100];
  double q_temps[MAXARRAY];

  gm_file_change(infilename,device);
  sprintf(sys_com,"spectre -E -info +warn +error %s",infilename);
  system(sys_com);
  get_temps(q_temps,size);
  return(new_calc_cost(q_temps,cost_devices,num_cost_devices));
}


void array_col_mult(double square[][MAXARRAY],double *column,int rows)
{
  int loop,loop1;
  double local_col[MAXARRAY];
```

```
  for(loop=0;loop<rows;loop++)
    {
      local_col[loop]=0.0;
      for(loop1=0;loop1<rows;loop1++)
     local_col[loop]+=square[loop][loop1]*column[loop1];
    }

  for(loop=0;loop<rows;loop++)
    column[loop]=local_col[loop];
}

void row_array_mult(double square[][MAXARRAY],double *row, int cols)
{
  int loop,loop1;
  double local_row[MAXARRAY];

  for(loop=0;loop<cols;loop++)
    {
      local_row[loop]=0.0;
      for(loop1=0;loop1<cols;loop1++)
     local_row[loop]+=row[loop1]*square[loop1][loop];
    }

  for(loop=0;loop<cols;loop++)
    row[loop]=local_row[loop];
}

void col_row_mult(double square[][MAXARRAY],double *col,double *row,
```

```
int cols)
{
  int loop,loop1;

  for(loop=0;loop<cols;loop++)
    for(loop1=0;loop1<cols;loop1++)
      square[loop][loop1]=col[loop]*row[loop1];
}

double row_col_mult(double *row,double *col,int rows)
{
  int loop;
  double return_val=0.0;

  for(loop=0;loop<rows;loop++)
    return_val+=row[loop]*col[loop];

  return(return_val);
}

void array_array_mult(double square1[][MAXARRAY],double square2[]
[MAXARRAY],int rows)
{
  int loop,loop1,loop2;
  double result_array[MAXARRAY][MAXARRAY];

  for(loop=0;loop<rows;loop++)
    for(loop1=0;loop1<rows;loop1++)
      {
```

```
     result_array[loop][loop1]=0.0;
     for(loop2=0;loop2<rows;loop2++)
       result_array[loop][loop1]+=square1[loop][loop2]*square2[loop2]
       [loop1];
      }

  for(loop=0;loop<rows;loop++)
    for(loop1=0;loop1<rows;loop1++)
      square1[loop][loop1]=result_array[loop][loop1];
}

void array_scalar_mult(double square[][MAXARRAY],double scalar,
int rows)
{
  int loop,loop1;

  for(loop=0;loop<rows;loop++)
    for(loop1=0;loop1<rows;loop1++)
      square[loop][loop1]*=scalar;
}

void array_array_add(double square1[][MAXARRAY],double square2[]
[MAXARRAY],int rows)
{
  int loop,loop1;

  for(loop=0;loop<rows;loop++)
    for(loop1=0;loop1<rows;loop1++)
      square1[loop][loop1]+=square2[loop][loop1];
```

```
}


double newton_derivatives(char *infilename,double h[][MAXARRAY],
double *n,struct transistor *device,int num_gaps,int num_devices,
 struct transistor *cost_devices,struct gaps *all_gaps,
int num_cost_devices,double delta)
{
  double base_cost,local_n[MAXARRAY],local_spacing[MAXARRAY],
  local_spacing1[MAXARRAY],deriv_cost,dev_loop,dev_loop1;
  int loop,loop1,loop2,v_gap;
  struct transistor local_device[MAXARRAY];

  base_cost=get_cost(infilename,device,num_devices,cost_devices,
  num_cost_devices);
  for(loop=0;loop<num_gaps;loop++)
    {
      for(loop1=0;loop1<num_devices;loop1++)
     {
       strcpy(local_device[loop1].name,device[loop1].name);
       local_device[loop1].x=device[loop1].x;
       local_device[loop1].y=device[loop1].y;
     }
      new_update_pos(local_device,all_gaps,num_devices,loop,delta);
      deriv_cost=get_cost(infilename,local_device,num_devices,cost_devices,
      num_cost_devices);
      n[loop]=(deriv_cost-base_cost)/delta;
```

```
      for(loop1=0;loop1<num_devices;loop1++)
    {
      strcpy(local_device[loop1].name,device[loop1].name);
      local_device[loop1].x=device[loop1].x;
      local_device[loop1].y=device[loop1].y;
    }
      new_update_pos(local_device,all_gaps,num_devices,loop,-delta);
      deriv_cost=get_cost(infilename,local_device,num_devices,cost_devices,
      num_cost_devices);
      local_n[loop]=(base_cost-deriv_cost)/delta;

      h[loop][loop]=(n[loop]-local_n[loop])/delta;
   }

for(loop=1;loop<num_gaps;loop++)
  for(loop1=0;loop1<loop;loop1++)
    {
      for(loop2=0;loop2<num_devices;loop2++)
    {
      strcpy(local_device[loop2].name,device[loop2].name);
      local_device[loop2].x=device[loop2].x;
      local_device[loop2].y=device[loop2].y;
    }

      new_update_pos(local_device,all_gaps,num_devices,loop,delta);
      new_update_pos(local_device,all_gaps,num_devices,loop1,delta);
      deriv_cost=get_cost(infilename,local_device,num_devices,cost_devices,
      num_cost_devices);
```

```
       dev_loop=(deriv_cost-(n[loop]*delta+base_cost))/delta;
       dev_loop1=(deriv_cost-(n[loop1]*delta+base_cost))/delta;

       h[loop][loop1]=(dev_loop-n[loop1])/delta;
       h[loop1][loop]=h[loop][loop1];
      }

  return(base_cost);
}

void get_seeds(char *infile,double *spacing,double *v_spacing,
int space_size)
{
  int seed=0,loop;
  char infileline[255];
  FILE *seedfile;

  seedfile=fopen(infile,"r");
  while(get_ln(infileline,seedfile))
    {
      loop=0;
      while(loop<strlen(infileline))
     {
       while(isspace(infileline[loop]))
         loop++;
       if(loop<strlen(infileline))
         {
           if(seed<space_size)
          spacing[seed]=atof(infileline+loop);
```

```
            else
           v_spacing[seed-space_size]=atof(infileline+loop);
            seed++;
            while(!isspace(infileline[loop])&&loop<strlen(infileline))
           loop++;
          }
     }
    }

  fclose(seedfile);
}

#define NUMQ 6 //Actually number of Q gaps total
#define NUMGAP 3 //
Number of optimized gaps (with ends being left at min space)

int main(int argc, char *argv[ ])
{
     FILE *infile,*outfile;
     char infilename[100],outfilename[100],seedfilename[100];
     char infileline[255],infilestrings[100][100],sys_com[100];
     int num_strings,loop,loop1,loop_remain,q_count=0,q_flag,g_count,
     dev1,dev2,dev_count,cost_loop;
     int h_size,dev_loop1,dev_loop2,dev_loop3,dev_loop4,num_gap,num_q=
     NUMQ,casc_flag=0,v_gap,seed_flag=0;
     double min_dist=2.0,gm=.00002,q_spacing[MAXARRAY],delta=.0015;
     double cost_values[3][3][3],space1,space2,space3;
     double h_array[MAXARRAY][MAXARRAY],n_col[MAXARRAY],n_col1[MAXARRAY]
     ,temp_col[MAXARRAY];
```

```
double x_col[MAXARRAY],x_col1[MAXARRAY],v_spacing[MAXARRAY+1];
double q_temps[MAXARRAY+1],fib_min,global_cost;

struct transistor devices[MAXARRAY],cost_devices[MAXARRAY];
struct gaps all_gaps[MAXARRAY];
int num_devices,num_gaps,num_cost_devices;
double thresh;



if(argc<3)
  {
  printf("usage: %s seedfilename infilename thresh\n",argv[0]);
  exit(0);
  }
else
  {
    strcpy(seedfilename,argv[1]);
    strcpy(infilename,argv[2]);
     thresh=atof(argv[3]);
    strcpy(outfilename,"temp.out");
  }

infile=fopen(seedfilename,"r");
read_q_file(infile,devices,cost_devices,all_gaps,&num_devices,
&num_gaps,&num_cost_devices);
fclose(infile);

global_cost=thresh+1;
```

```
while(global_cost>=thresh)
  {
    global_cost=newton_derivatives(infilename,h_array,n_col,devices,
    num_gaps,num_devices,cost_devices,all_gaps,num_cost_devices,delta)
    ;

    inverse(h_array,num_gaps);
    array_col_mult(h_array,n_col,num_gaps);

    printf("%lg\n",global_cost);
    for(loop=0;loop<num_gaps;loop++)
      printf("%lg\t",n_col[loop]);
    printf("\n");

    for(loop=0;loop<num_gaps;loop++)
      {
     new_update_pos(devices,all_gaps,num_devices,loop,-n_col[loop])
     ;
      }


    loop1=0;
    while(loop1<num_gaps&&all_gaps[loop1].type=='X')
      loop1++;

    if(loop1==num_gaps)
      for(loop=0;loop<num_devices-1;loop++)
     printf("%lg\t",devices[loop+1].x-devices[loop].x);
    else
```

```
            {
            for(loop=1;loop<num_devices;loop+=2)
              printf("%lg\t",devices[loop].y);
            printf("\n");

            for(loop=0;loop<num_devices-2;loop+=2)
              printf("%lg\t",devices[loop+2].x-devices[loop].x);
             }

          printf("\n\n");

        }
}
```

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